Sunday, 13 April

9am	**Educational Session 1: Mastering LLMs: A Deep Dive into Software Models, Hardware Challenges, Security and Reliability** *Olympia* Chaired by: Shanshan Xie (United States) and Prof. Yoonmyung Lee (Korea, Republic of)
9am	**ES1-1: Enabling Generative AI on Mobile SoCs using Hardware-Model Co-Design** » Dr. Paul Whatmough (United States)[1] (1. Qualcomm)
10:45am	**ES1-2: Breaking the Resource Monopoly from Industries: Sustainable and Reliable LLM Serving By Recycling Outdated and Resource-Constrained GPUs** » Dr. Tianlong Chen (United States)[1] (1. Assistant Professor at The University of North Carolina at Chapel Hill)
9am	**Educational Session 2: High Precision Converters and Digital Calibration Techniques** *Michelangelo* Chaired by: Prof. Shaolan Li (United States) and Dr. Yong Liu (United States)
9am	**ES2-1: Noise-Shaping SAR ADCs: From Fundamentals to Recent Advances** » Prof. Xiyuan Tang (China)[1] (1. Peking University)
10:45am	**ES2-2: ADC Architectures and Techniques for Biomedical and Sensor Interfaces** » Prof. Minkyu Je (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology)
9am	**Educational Session 3: Security or Privacy From Hardware to Systems** *Aquitania* Chaired by: Dr. Kevin Tien (United States)
9am	**ES3-1: Bringing the zero-trust model to hardware: From systems to silicon** » Dr. Sandhya Koteshwara (United States)[1] (1. IBM)
10:45am	**ES3-2: Attack-Resistant Crypto Hardware Accelerators for Secure Platforms** » Dr. Sanu Mathew (United States)[1] (1. Intel Corporation)
9am	**Educational Session 4: Advanced Biomedical Interfaces** *Brittannic* Chaired by: Prof. Constantine Sideris (United States) and Dr. Yaoyao Jia (United States)
9am	**ES4-1: Efficient and Effective Implantable Neural Stimulation: Challenges and Circuit Solutions** » Prof. Hyung-Min Lee (Korea, Republic of)[1] (1. Korea University)
10:45am	**ES4-2: On-chip signal processing and compression for brain-computer interfaces** » Prof. Dante Gabriel Muratore (Netherlands)[1] (1. Delft University of Technology)
9:15am	**Circuits Insights I - Circuits Insights** *Grand Ballroom*
12pm	**Circuits Insights II - Networking Lunch** *Grand Ballroom*
12:15pm	**Lunch Break (on own)**
1:30pm	**Educational Session 1: Mastering LLMs: A Deep Dive into Software Models, Hardware Challenges, Security and Reliability** *Olympia* Chaired by: Prof. Yoonmyung Lee (Korea, Republic of) and Shanshan Xie (United States)

Continued from **Sunday, 13 April**

1:30pm **ES1-3: Deploying LLMs on the Edge: A HW/SW Co-Design Perspective**
» Dr. Debabrata Mohapatra (United States)[1] (1. Meta)

3:15pm **ES1-4: LLM Innovation with User Data**
» Prof. Xiaozhong Liu (United States)[1] (1. Associate Professor at Worcester Polytechnic Institute)

1:30pm **Educational Session 2: High Precision Converters and Digital Calibration Techniques**
Michelangelo
Chaired by: Dr. Yong Liu (United States) and Prof. Shaolan Li (United States)

1:30pm **ES2-3: Continuous-Time Delta-Sigma Modulators Architectures**
» Prof. Nima Maghari (United States)[1] (1. University of Florida)

3:15pm **ES2-4: Background Calibration Techniques for High-Speed Pipelined ADCs**
» Dr. Huseyin Dinc (United States)[1] (1. ADI)

1:30pm **Educational Session 3: Security or Privacy From Hardware to Systems**
Aquitania
Chaired by: Dr. Kevin Tien (United States)

1:30pm **ES3-3: Securing Ubiquitous Devices with Ultra-Lightweight Circuit Primitives**
» Prof. Kaiyuan Yang (United States)[1] (1. Rice University)

3:15pm **ES3-4: Reuse-Centric Design for Ubiquitous Hardware Security - From Circuits to Machine Learning Algorithms**
» Prof. Massimo Alioto (Singapore)[1] (1. Department of Electrical and Computer Engineering, National University of Singapore)

1:30pm **Educational Session 4: Advanced Biomedical Interfaces**
Brittannic
Chaired by: Dr. Yaoyao Jia (United States) and Prof. Constantine Sideris (United States)

1:30pm **ES4-3: Wireless Power Transfer to Implantable Medical Devices**
» Prof. Mehdi Kiani (United States)[1] (1. Penn State University)

3:15pm **ES4-4: Wearable e-health: from electrodes to signal processing and powering**
» Prof. Jerald Yoo (Korea, Republic of)[1] (1. Seoul National University)

1:30pm **Circuits Insights III - Circuit Insights**
Grand Ballroom

5pm **SSCS Bingo Networking Night**
Skyline Ballroom
Chaired by: SSCS Women in Circuits

Monday, 14 April

8:30am **Welcome and Opening Remarks**
Grand Ballroom

8:50am **Session 1: Keynote Session**
Grand Ballroom

8:50am **AI at the Edge: Notes From the Field**
» Dr. Scott Hanson (United States)[1] (1. Chief Technology Officer, Founder, Ambiq)

9:40am **Break**
Grand Ballroom Foyer

Continued from **Monday, 14 April**

10:05am **Analog Circuits and Techniques I -**
Session 2: Analog Building Blocks and Sensing Circuits
Grand Ballroom
Chaired by: Chilun Lo (United States) and Soo Youn Kim (Korea, Republic of)

10:05am **2-1: A direct digitizing, 1MHz bandwidth, 28fA/√Hz current sensing front-end based on a mixed-signal integrator-differentiator TIA in 28nm CMOS**
» Mr. David-Peter Wiens (Germany)[1], Mr. Ahmed Abdelaal (Germany)[1], Mr. Bjoern Driemeyer (Germany)[1], Dr. Joachim Becker (Germany)[1], Dr. John Kauffman (Germany)[1], Prof. Maurits Ortmanns (Germany)[1] (1. University of Ulm)

10:30am **2-2: A 0.6V Supply Ultra-Compact Voltage Reference Exploiting MOS Threshold Correlations**
» Dr. Matthias Eberlein (Germany)[1], Mr. Sebastian Rupping (Germany)[1] (1. Fraunhofer EMFT)

10:55am **2-3: A 16 GΩ input impedance amplifier with flicker noise reduction for neural recording applications**
» Dr. Jyotindra Shakya (United States)[1], Mr. Faraz Adin (United States)[1], Prof. Gabor Temes (United States)[1] (1. Oregon State University)

11:20am **2-4: Multi-electroanalytical method capable, duty-cycled, 0.36 mm2 electrochemical frontend, achieving 170dB current sensing range with extended compliance voltage adopting feedforward cancellation**
» Dr. Amrith Sukumaran (Switzerland)[1], Mr. Francesco CARUSO (Switzerland)[1], Mr. Régis CATTENOZ (Switzerland)[1], Mr. Bas PUTTER (Switzerland)[1], Mr. Jean-Luc NAGEL (Switzerland)[1], Mr. Renil RAVANILLA (Switzerland)[1], Mr. IOANNIS STERGIOU (Switzerland)[1], Mr. Guillaume BOUILLY (Switzerland)[1], Mr. Pascal NUSSBAUM (Switzerland)[1], Mr. Stéphane EMERY (Switzerland)[1] (1. CSEM)

11:45am **2-5: A 14-Cell Battery Monitoring AFE with 1mV Total Measurement Error and Integrated Electrochemical Impedance Spectroscopy**
» Mr. Xining Zhang (China)[1], Mr. Yuxiang Tang (China)[1], Mrs. Yaohua Pan (China)[2], Mr. Wenhui Qin (China)[2], Mr. Jian Ye (China)[2], Dr. Shaoyu Ma (China)[2], Mr. Yun Sheng (China)[2], Prof. Zhiliang Hong (China)[1], Prof. Jiawei Xu (China)[1] (1. Fudan University, 2. Novosense Microelectronics)

10:05am **Wireless Transceivers and RF/mm-Wave Circuits and Systems I -**
Session 3: Voltage Controlled Oscillators and Power Amplifiers
Olympia
Chaired by: Hamed Rahmani (United States) and Padmanava Sen (Germany)

10:05am **3-1: A 28-GHz 189.2-dBc/Hz FoM 360° Phase-Shifting Quadrature Oscillator Without Phase Ambiguity Achieving 0.13° RMS Phase Error Under 2° Phase Resolution**
» Mr. Hongkun Li (China)[1], Dr. Yiyang Shu (China)[1], Prof. Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

10:30am **3-2 (BEST STUDENT PAPER CANDIDATE): A 4.6-6GHz Self-Injection LC Oscillator Exploiting 2nd Harmonic Extraction and Self-Mixing to Achieve 5-35kHz 1/f3 Phase Noise Corner and 201dB FoMT**
» Mr. Bahram Jafari Akinabad (Canada)[1], Dr. Sankaran Aniruddhan (India)[2], Dr. Shahriar Mirabbasi (Canada)[1], Dr. Sudip Shekhar (Canada)[1] (1. University of British Columbia, 2. Indian Institute of Technology Madras)

10:55am **3-3 (BEST STUDENT PAPER CANDIDATE): A 104-to-132 GHz 16-way Power Amplifier Using Enhanced Magnetic Coupling Cavity Achieving 21.2 dBm Output Power in 28nm Bulk CMOS**
» Mr. Ziyuan Guo (China)[1], Prof. Wei Deng (China)[1], Mr. Weiqi Zheng (China)[1], Prof. Haikun Jia (China)[1], Mr. Hongliang Wu (China)[1], Mr. Qiuyu Peng (China)[1], Dr. Fuyuan Zhao (China)[1], Mr. Junyang Yin (China)[1], Dr. Dongze Li (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

Continued from **Monday, 14 April**

11:20am

3-4: An Ultra-Compact Wideband-Linearized Power Amplifier Achieving 0.24° AM-PM Distortion and Supporting 64-/256-/1024-/4096-QAM

» Dr. Jingshang Dong (China)[1], Prof. Pei Qin (China)[1], Prof. Haoshen Zhu (China)[1], Prof. Xiang Yi (China)[1], Prof. Wenjie Feng (China)[1], Prof. Wenquan Che (China)[1], Prof. Quan Xue (China)[1], Mr. Ziyuan Guo (China)[2] (1. South China University of Technology, 2. Tsinghua University)

10:05am

Power Management I -
Session 4: SC-based Power Conversion
Michelangelo
Chaired by: Alan Roth (United States) and Min-Woo Ko (Canada)

10:05am

4-1 (BEST REGULAR PAPER CANDIDATE): An SC-first Hybrid SCVR with 4xCF Continuously Scalable-Conversion Ratio SC Achieving 92.5% Peak Efficiency

» Dr. Yuanfei Wang (Macao)[1], Mr. Zhiyuan Zhang (Macao)[1], Mr. Ziyang Zhong (Macao)[1], Prof. Yihan Zhang (Hong Kong)[2], Prof. Rui P. Martins (China)[1], Prof. Mo Huang (Macao)[1] (1. University of Macau, 2. Hong Kong University of Science and Technology)

10:30am

4-2: A LEGO-Like Easy-Stacking Step-Up SC Converter with Ultra-High and Wide VCR Using All Input-Stress-Only Devices

» Dr. Shousheng Han (China)[1], Mr. Fei Song (China)[2], Mr. Zhongyao Zhu (China)[2], Prof. Xiaoming Wu (China)[3], Prof. Hanjun Jiang (China)[3], Prof. Tianling Ren (China)[3], Prof. Yan Lu (China)[3] (1. Tsinghua University and University of Macau, 2. University of Macau, 3. Tsinghua University)

10:55am

4-3: A 5V-Input, 12.5-to-45V-Output Reconfigurable Hybrid Boost Converter with an SC-Based Parallel Auxiliary Cell Achieving 96.8% Peak Efficiency

» Dr. Gyeong-Gu Kang (United States)[1], Prof. Minjie Chen (United States)[1], Prof. Hyun-Sik Kim (Korea, Republic of)[2] (1. Princeton University, 2. KAIST)

11:20am

4-4: A 6.87W 3.7-5V Input 12.6-24V Output Switched-Capacitor Sigma Converter with Multiple Voltage Domains

» Mr. Lingfeng Zhu (China)[1], Dr. Chen Hu (China)[1], Prof. Wing Hung Ki (Hong Kong)[2], Dr. Xun Liu (China)[3], Prof. Xiaosen Liu (China)[4], Prof. Junmin Jiang (China)[1] (1. Southern University of Science and Technology, 2. Hong Kong University of Science and Technology, 3. Chinese University of Hong Kong, 4. Tsinghua University)

10:05am

Data Converters I -
Session 5: Incremental ADCs
Aquitania
Chaired by: Prof. Sai-Weng Sin (Macao) and Yong Lim (Korea, Republic of)

10:05am

5-1: (INVITED) Reducing the Impact of Non-Idealities on Incremental Delta-Sigma ADCs by Reconfiguration: A Review

» Mr. Omar Ismail (Germany)[1], Mr. Paul Kaesser (Germany)[1], Prof. Maurits Ortmanns (Germany)[1] (1. University of Ulm)

10:55am

5-2: A 133.6-µW 1kHz-BW Multi-bit 2nd-order Incremental ADC Achieving 115.4-dB SNDR with Low-Cost Coarse-Sorting DEM and Zip Extended-Counting

» Mr. Yajie Zhao (China)[1], Mr. Yongjie Ye (China)[1], Mr. Shaokai Yuan (China)[1], Prof. Yajie Qin (China)[1] (1. Fudan University)

11:20am

5-3: A 16-bit Incremental ADC Enabled by An Efficient Shooting Integrator with Inherent Noise Reduction

» Dr. Bo Wang (Qatar)[1], Prof. Amine Bermak (Qatar)[1], Prof. Man-Kay Law (Macao)[2] (1. Hamad Bin Khalifa University, 2. University of Macau)

11:45am

5-4 (BEST STUDENT PAPER CANDIDATE): A 50-kHz BW 92.1-dB SNDR Incremental ADC Using a Back-End Sampling Two-Step NS-SAR Architecture with Concurrent Gain-Error + Noise Suppression

» Mr. Tzu-Han Wang (United States)[1], Mr. Chenyang Li (United States)[1], Mr. Dong-Suk Kang (United States)[1], Mr. Ken Li (United States)[1], Mr. Xitie Zhang (United States)[1], Mr. Wei-En Lee (United States)[1], Prof. Visvesh Sathe (United States)[1], Prof. Shaolan Li (United States)[1] (1. Georgia Institute of Technology)

Continued from **Monday, 14 April**

10:05am **Digital Circuits and SoCs I -**
Session 6: Forum: Hardware and Architectural Strategies for Building Cutting-edge AI Platforms
Brittannic
Chaired by: Sumanth Kamineni (United States) and Prof. Visvesh Sathe (United States)

12pm **Lunch Break (on own)**

1:30pm **Analog Circuits and Techniques II -**
Session 7: Panel: Do we really need a linear-gain amplifier anymore?
Grand Ballroom
Chaired by: Anne-Johan Annema (Netherlands) and Devrim Aksin (United States)

1:30pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems II -**
Session 8: Advancements in Low-Power Wireless Technologies
Olympia
Chaired by: Tong Zhang (United States) and Najme Ebrahimi (United States)

1:30pm **8-1: A 0.5V 0.55mm2 Bias-Current-Free BLE Transceiver With 1-Bit Delay-Based Demodulation for Energy-Harvesting IoT Applications**
» Mr. Liqun Feng (China)[1], Mr. Xuansheng Ji (China)[1], Ms. Qianxian Liao (China)[1], Mr. Longhao Kuang (China)[1], Mr. Yunzhao Nie (China)[1], Dr. Jiahao Zhao (China)[1], Prof. Woogeun Rhee (China)[1], Prof. Zhihua Wang (China)[1] (1. Tsinghua University)

1:55pm **8-2: A Passive Crystal-Less Tag Demonstrating Battery-Free GSM-CW/5G-NR Downlink and BLE-to-BLE/BLE-to-WiFi/WiFi-to-WiFi Multi-Channel-Hopping Uplink with Smartphones**
» Mr. Qijing Xiao (China)[1], Dr. Changgui Yang (China)[2], Dr. Yunshan Zhang (China)[2], Dr. Ziyi Chang (China)[1], Mr. Cheng Chen (China)[2], Mr. Xin Hu (China)[1], Mr. Weixiao Wang (China)[1], Mr. Guanjie Gu (China)[1], Prof. Yuxuan Luo (China)[1], Prof. Bo Zhao (China)[1] (1. Zhejiang University, 2. Microaiot)

2:20pm **8-3: D-band Dicke switch based Passive Imager with 0.13K NETD in 28nm CMOS Technology**
» Ms. Zahra Mohseni (United States)[1], Mr. Sajjad Sabbaghi (United States)[1], Dr. Hai Yu (United States)[2], Mr. Peixin Han (United States)[3], Prof. Q. Gu (United States)[1] (1. Georgia Institute of Technology, 2. NVIDIA Corporation, 3. University of California, Davis)

2:45pm **8-4: A 1.8Gb/s 8GHz PSK-UWB Transceiver with Extended PPM/PWM Modulation and Embedded Carrier Spreading**
» Ms. Luhua Lin (China)[1], Dr. Bowen Wang (China)[1], Mr. Longhao Kuang (China)[1], Prof. Woogeun Rhee (China)[1], Prof. Zhihua Wang (China)[1] (1. Tsinghua University)

1:30pm **Power Management II -**
Session 9: Power Converter Techniques
Michelangelo
Chaired by: Raveesh Magod (United States) and Edevaldo Pereira (United States)

1:30pm **9-1: A 30V Step-Up Regulator with Shunt-Current-Reuse Controller for >85% Efficiency over 200μA-100mA Loading Range**
» Dr. Yue Zhao (China)[1], Mr. Pengda Qu (China)[1], Dr. Guangshu Zhao (Macao)[2], Prof. Feng Luo (China)[1], Prof. Yang Jiang (Macao)[2], Prof. Zhiming Xiao (China)[1], Mr. Xiongjie Zhang (Macao)[2] (1. Nankai University, 2. University of Macau)

1:55pm **9-2: A Fast-transient Buck Converter with One-Cycle-Balancing Control for Single and Consecutive Load Steps**
» Mr. Zihao Tang (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Mo Huang (Macao)[1] (1. University of Macau)

2:20pm **9-3: A Pseudo-4-Phase Buck Converter with 94.1% Efficiency, 1mV Output Ripple and Fast Transient Response**
» Mr. Yu-Chen Kuo (Taiwan)[1], Mr. Yu-Ting Huang (Taiwan)[1], Prof. Ke-Horng Chen (Taiwan)[1], Mr. Kuo-Lin Zheng (Taiwan)[2], Mr. Ying-Hsi Lin (Taiwan)[3], Mr. Shian-Ru Lin (Taiwan)[3], Mr. Tsung-Yen Tsai (Taiwan)[3], Prof. Xi Zhu (Australia)[4] (1. National Yang Ming Chiao Tung University, 2. Chip-GaN Semiconductor Company, 3. Realtek Semiconductor, 4. University of Technology Sydney)

Continued from **Monday, 14 April**

2:45pm

9-4: A 300-kHz 3-Level Flyback Converter Achieving 93% Peak Efficiency and 50% Reduction in Transformer Size

» Mr. Yuanzhuo Wu (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Mo Huang (Macao)[1] (1. University of Macau)

1:30pm

Emerging Technology I -
Session 10: Emerging Paradigms for AI, HPC, and Edge Computation

Aquitania

Chaired by: Dr. Kevin Tien (United States) and Tathagata Srimani (United States)

1:30pm

10-1: (INVITED) Analog-AI Hardware Accelerators for low-latency Transformer-based Language Models (Invited)

» Dr. Geoffrey W. Burr (United States)[1], Dr. Hsinyu Tsai (United States)[1], Dr. Irem Boybat (Switzerland)[2], Dr. William A. Simon (Switzerland)[2], Mr. Julian Büchel (Switzerland)[2], Mr. Athanasios Vasilopoulos (Switzerland)[2], Dr. Pritish Narayanan (United States)[1], Dr. Andrea Fasoli (United States)[1], Mr. Kohji Hosokawa (Japan)[3], Dr. Manuel Le Gallo (Switzerland)[2], Mr. Masatoshi Ishii (Japan)[3], Mr. Yasuteru Kohda (Japan)[3], Mr. Atsuya Okazaki (Japan)[3], Dr. An Chen (United States)[1], Dr. Charles Mackin (United States)[1], Ms. Elena Ferro (Switzerland)[2], Dr. Kaoutar El Maghraoui (United States)[4], Dr. Hadjer Benmeziane (Switzerland)[2], Dr. Timothy Philicelli (United States)[5], Dr. Corey Lammie (Switzerland)[2], Mr. Alexander M. Friz (United States)[1], Mr. Jose Luquin (United States)[1], Dr. Shubham Jain (United States)[4], Dr. Abu Sebastian (Switzerland)[2], Dr. Vijay Narayanan (United States)[4] (1. IBM Research - Almaden, 2. IBM Research Europe, 3. IBM Tokyo Research Laboratory, 4. IBM T. J. Watson Research Center, 5. IBM Albany Nanotech)

2:20pm

10-2 (BEST STUDENT PAPER CANDIDATE): A Reconfigurable Potts Machine with Successive Boundary Approximation Annealing for Solving Combinatorial Optimization Problems

» Dr. Yifeng Zhou (China)[1], Mr. Xin Hao (China)[1], Mr. Qinchao Cai (China)[1], Prof. Lei Liao (China)[1], Prof. Zhuojun Chen (China)[1] (1. Hunan University)

2:45pm

10-3: 16 Arrays of 32 All-to-all Coupled CMOS Oscillators for AI Inference and Combinatorial Optimization

» Dr. Hai Li (United States)[1], Dr. James Ayers (United States)[1], Dr. Anni Lu (United States)[1], Dr. You Li (United States)[1], Dr. Dmitri Nikonov (United States)[1], Dr. Yongping Fan (United States)[1], Dr. Ian Young (United States)[1] (1. Intel Corporation)

1:30pm

Digital Circuits and SoCs II -
Session 11: ASIC and Accelerators

Brittannic

Chaired by: Muya Chang and Divya Prasad

1:30pm

11-1 (BEST STUDENT PAPER CANDIDATE): An 209TOPS/W Reinforcement Learning Processor with Full Speculation Exploitation and Inference-Training Parallel Processing

» Mr. Shih-Hao Chen (Taiwan)[1], Mr. Ping-Sheng Wu (Taiwan)[1], Mr. Brian Dean Soon (Taiwan)[1], Mr. Chao-Hung Chen (Taiwan)[2], Mr. Chih-Wei Liu (Taiwan)[2], Mr. Chun-Lung Hsu (Taiwan)[2], Prof. Chia-Hsiang Yang (Taiwan)[1] (1. National Taiwan University, 2. Industrial Technology Research Institute)

1:55pm

11-2: AJPEG: A 26.4-pJ/pixel, 252-fps, 128x128 Image Sensor with an In-Sensor Analog DCT Processor for Data Compression

» Mr. Rentao Wan (United States)[1], Mr. Yichen Xu (United States)[1], Prof. Dong-Woo Jee (Korea, Republic of)[2], Prof. Mingoo Seok (United States)[1] (1. Columbia University, 2. Ajou University)

2:20pm

11-3: SparseTrim: A Neural Network Accelerator Featuring On-Chip Decompression of Fine-Grained Sparse Model with 10.1TOPS/W System Energy Efficiency

» Ms. Jieyu Li (China)[1], Prof. Weifeng He (China)[1], Mr. Boran Jiang (China)[1], Mr. Xinyu Wang (China)[1], Prof. Guanghui He (China)[1], Mr. Dingxuan Liu (China)[2], Prof. Mingoo Seok (United States)[3] (1. Shanghai Jiao Tong University, 2. Aicxtek Technologies Co., Ltd., 3. Columbia University)

2:45pm

11-4: Aspen: A 630 FPS Real-Time Posit-Based Unified Accelerator for Extended Reality Perception Workloads

» Ms. Kathleen Feng (United States)[1], Mr. Kartik Prabhu (United States)[1], Mr. Kai Bartolone (United States)[1], Mr. Jeffrey Yu (United States)[1], Prof. Priyanka Raina (United States)[1] (1. Stanford University)

Continued from **Monday, 14 April**

3:10pm **Break**
Grand Ballroom Foyer

3:35pm **Analog Circuits and Techniques III -**
Session 12: Advancements in Low-Power, High-Performance Analog Sensing and Interface Technologies
Grand Ballroom
Chaired by: Prof. Edoardo Bonizzoni (Italy) and Prof. Linxiao Shen (China)

3:35pm **12-1: (INVITED) Recording Front-End Electronics for Large-Scale Implantable Brain-Computer Interfaces: A Design Perspective**
» Dr. Xiaohua Huang (Netherlands)[1], Prof. Dante Gabriel Muratore (Netherlands)[1] (1. Delft University of Technology)

4:25pm **12-2: A 4.82-µW 183.4dB-FoMSNDR CT Incremental Tracking-Zoom Sensor Readout Frontend with Floating-Gm-CCO Integrator**
» Mr. Haoyang Luo (China)[1], Mr. Zongnan Wang (China)[1], Mr. Jiarui Wang (China)[1], Mr. Bingrui Li (China)[1], Dr. Zilong Shen (China)[1], Ms. Yang Liu (China)[1], Prof. Xiaojie Duan (China)[1], Prof. Yuan Wang (China)[1], Prof. Xiyuan Tang (China)[1] (1. Peking University)

4:50pm **12-3 (BEST STUDENT PAPER CANDIDATE): A Fully-Dynamic Capacitive Touch Sensor with Tri-level Energy Recycling and Compressive Sensing Technique Achieving 1513 Hz Framerate and 10.66 pJ/step Energy Efficiency**
» Mr. Xiangdong Feng (China)[1], Mr. zhiyu wang (China)[1], Mr. Haoyang Li (China)[1], Mr. Jiaqing Li (China)[1], Mr. Guanglong Wu (China)[2], Mr. Wei Wang (China)[2], Mr. Weijin Lin (China)[1], Mr. Xin Hu (China)[1], Mr. Weixiao Wang (China)[1], Mr. Zhong Tang (China)[3], Mr. Yuyan Liu (Netherlands)[4], Mr. Qinwen Fan (Netherlands)[4], Mr. Hua Liu (China)[5], Mr. Jianqiu Chen (China)[5], Prof. Yuxuan Luo (China)[1], Prof. Bo Zhao (China)[1] (1. Zhejiang University, 2. Microaiot, 3. Vango Technologies, 4. Delft University of Technology, 5. Shanghai Hynitron Technology Co.,Ltd)

3:35pm **Data Converters II -**
Session 13: High-Speed Nyquist ADCs
Olympia
Chaired by: Thomas Brown (United States) and Haiyang (Henry) Zhu (United States)

3:35pm **13-1 (BEST STUDENT PAPER CANDIDATE): A Timing-Robust 10b 13GS/s ADC with Analog Fourier Transform Based Frequency Interleaving**
» Mr. Xingchen Chao (China)[1], Mr. Yunqiang Xu (China)[1], Mr. Qiang Yu (China)[1], Mr. Zheng Zhu (China)[2], Dr. Sanfeng Zhang (China)[2], Prof. Qiang Li (China)[1] (1. University of Electronic Science and Technology of China, 2. Voyager Technologies)

4pm **13-2: A 12.5GS/s 14.7mW 4×TI Pipelined Hybrid TD-SAR ADC with Residual Time-Voltage Amplification**
» Mr. Haoyu Li (Macao)[1], Mr. Boyang Wang (Macao)[1], Mr. Hongjiang Chen (Macao)[1], Prof. Sai-Weng Sin (Macao)[1], Mr. Yutao Peng (China)[2], Prof. Xizhu Peng (China)[2], Prof. He Tang (China)[2], Prof. Chao Fan (China)[3], Prof. Liang Qi (China)[4], Prof. Rui P. Martins (China)[1], Prof. Mingqiang Guo (Macao)[1] (1. University of Macau, 2. University of Electronic Science and Technology of China, 3. Xi'an Jiaotong University, 4. Shanghai Jiao Tong University)

4:25pm **13-3: A 13b 2GS/s Time-Domain Pipelined ADC with Split-CDAC Ping-Pong Residue Transfer and PVT-Robust Self-Tracked Time Amplifier**
» Dr. Xin Zhao (China)[1], Prof. Dengquan Li (China)[1], Mr. Feida Wang (China)[1], Mr. Depan Li (China)[1], Prof. Yi Shen (China)[1], Dr. Hongzhi Liang (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

4:50pm **13-4: A 32GS/s 8b 16× Time-interleaved Hybrid ADC with Self-Detection Offset Calibration, DLL-Based TLSB PVT Variation Calibration and VTC Gain Self-Tracking.**
» Dr. Hongzhi Liang (China)[1], Dr. Jun Chang (China)[1], Dr. Yixiao Luo (China)[1], Dr. Zeyu Peng (China)[1], Mr. Weimin Zhou (China)[1], Dr. Li Dang (China)[1], Dr. Yue Cao (China)[1], Dr. Haolin Han (China)[1], Prof. Yi Shen (China)[1], Prof. Shubin Liu (China)[1], Prof. Ruixue Ding (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

Continued from **Monday, 14 April**

5:15pm

13-5: A 17.4fJ/conv.-step, 202µm^2, 1.5GS/s and PVT-Tolerant 7-bit Charge-Injection SAR ADC in 28nm CMOS Using a Background-Calibrated 1-bit Metastability Detector and a gm-Boosted StrongARM Comparator

» Ms. Chaeeun Lee (Korea, Republic of)[1], Dr. Jongho Kim (Korea, Republic of)[1], Prof. Jintae Kim (Korea, Republic of)[1] (1. Konkuk University)

3:35pm

Power Management II cont'd -

Session 9: Power Converter Techniques

Michelangelo

Chaired by: Raveesh Magod (United States) and Edevaldo Pereira (United States)

3:35pm

9-5: A Zero-Voltage-Switching Buck Converter with Conduction-Loss-Minimized ZVS Operation and Auxiliary Inductor Transient Reuse Technique Achieving up to 8.3% Efficiency Improvement and 42% Voltage Droop Reduction

» Ms. Qingqing Min (China)[1], Dr. Jingyi Yuan (China)[1], Prof. Lin Cheng (China)[1] (1. University of Science and Technology of China)

4pm

9-6: : A 96.1% Efficiency 48V-to-IBV GaN Power Converter with Full-Wave Temperature-Compensated Current Sensing and Adaptive Slope Emulation Achieving 4.3% Full-Temperature Sensing Error for AI Data Center Applications

» Mr. Yike Fang (China)[1], Mr. Wei He (China)[2], Mr. Jie Zou (China)[2], Prof. Xiang Gao (China)[1], Prof. Lenian He (China)[1], Prof. Xugang Ke (China)[1] (1. Zhejiang University, 2. Primechip Semiconductor)

4:25pm

9-7: A 25-nA Modified Hybrid Ladder Converter with Efficient Output-Capacitor Charge Recycling and 90% Battery Lifetime Extension

» Mr. jianxin yang (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Mo Huang (Macao)[1] (1. University of Macau)

4:50pm

9-8: An Up-to-70-V Output Hybrid Boost Converter with Halved Voltage Stress Achieving 7-W Output Power and 73.8% Peak Efficiency at CR of 14

» Mr. Dingxuan Zhang (China)[1], Mr. Tianrui Lyu (China)[1], Prof. Jianping Guo (China)[1] (1. Sun Yat-sen University)

3:35pm

Emerging Technology I cont'd -

Session 10: Emerging Paradigms for AI, HPC, and Edge Computation

Aquitania

Chaired by: Dr. Kevin Tien (United States) and Tathagata Srimani (United States)

3:35pm

10-4: (INVITED) Demonstration of Logic-Block Performance-Power-Area Gain by 1st Generation Back Side Power Delivery Network for SoC and HPC Applications beyond 2nm Node

» Dr. Hidenobu Fukutome (Korea, Republic of)[1], Mr. Jinkyu Kim (Korea, Republic of)[1], Mr. Jaehoon Shin (Korea, Republic of)[1], Mr. Jeewoong Kim (Korea, Republic of)[1], Dr. Yongwoo Lee (Korea, Republic of)[1], Mr. SOOHANG CHAE (Korea, Republic of)[1], Mr. Byeolhae Eom (Korea, Republic of)[1], Dr. YunSuk Nam (Korea, Republic of)[1], Dr. Minseung Lee (Korea, Republic of)[1], Dr. Seungseok Ha (Korea, Republic of)[1], Dr. EunGuk Chung (Korea, Republic of)[1], Dr. Seung Hun Lee (Korea, Republic of)[1], Dr. Sunjung Kim (Korea, Republic of)[1], Dr. Keun Hwi Cho (Korea, Republic of)[1], Dr. Kyoung Woo Lee (Korea, Republic of)[1], Dr. Dong-Won Kim (Korea, Republic of)[1], Dr. Hag-Ju Cho (Korea, Republic of)[1], Dr. Ken Rim (Korea, Republic of)[1], Dr. Jaihyuk Song (Korea, Republic of)[1] (1. Samsung Electronics)

4:25pm

10-5: A 40nm 4Mb High-Reliability STT-MRAM Achieving 18ns Write-Time and 94.9% Wafer-Level-Die-Yield across -55°C-to-125°C

» Mr. Yaoru HOU (China)[1], Mr. Haoran Du (China)[1], Mr. Jiongzhe Su (China)[1], Mr. Yibo Liu (China)[1], Mr. Zhenghan Fang (China)[1], Mr. Jiale Cui (China)[1], Mr. Shuyu Wang (China)[1], Ms. Chenxing Liu-sun (China)[1], Mr. Xuezhao Wu (Hong Kong)[2], Mr. Zhihua Xiao (Hong Kong)[2], Prof. Bo Liu (China)[1], Prof. Xin Si (China)[1], Prof. Jun Yang (China)[1], Prof. Qiming Shao (Hong Kong)[2], Prof. Hao Cai (China)[1] (1. southeast university, 2. Hong Kong University of Science and Technology)

Continued from **Monday, 14 April**

4:50pm **10-6: ISPI: A 2-Wire Improved Serial Peripheral Interface with Automatic Routing Algorithm for 2-D In-Textile Distributed Computing and Storage Systems**

» Mr. Zhenghong Chen (United States)[1], Mr. Braden Desman (United States)[1], Ms. Anjali Agrawal (United States)[1], Mr. Will Farrell (United States)[2], Mr. Jim Owens (United States)[2], Dr. Daniel Truesdell (United States)[1], Prof. Benton Calhoun (United States)[1] (1. University of Virginia, 2. Nautilus Defense LLC)

3:35pm **Digital Circuits and SoCs II cont'd - Session 11: ASIC and Accelerators**

Brittannic

Chaired by: Muya Chang and Divya Prasad

3:35pm **11-5: A 40nm 0.05-1.4uJ/inference Sample-Wise-Adaptive Spiking Neural Network Processor with Dynamic Neuron-Pruning and Unstructured-Model-Aware Architecture**

» Mr. Jinqiao Yang (China)[1], Mr. Zikai Zhu (China)[1], Ms. Longrun Xv (China)[1], Mr. Anqin Xiao (China)[1], Mr. Ziyi Yang (China)[1], Prof. Lirong Zheng (China)[1], Prof. Zhuo Zou (China)[1] (1. Fudan University)

4pm **11-6: A 28nm 3.14 TFLOPS/W BF16 LLM Fine-Tuning Processor with Asymmetric Quantization Computing for AI PC**

» Mr. Xinyuan Lin (China)[1], Mr. Leran Huang (China)[2], Mr. Chenhan Wei (China)[1], Mr. Wenbin Jia (China)[1], Mr. Hedi Wang (China)[1], Mr. Wenxun Wang (China)[1], Mr. Weichen Gao (China)[1], Prof. Hongyang Jia (China)[1], Prof. Sheng Zhang (China)[2], Prof. Huazhong Yang (China)[1], Prof. Yongpan Liu (China)[1] (1. Tsinghua University, 2. Tsinghua Shenzhen International Graduate School)

4:25pm **11-7: An 83.16-TOPS/W Voltage-Scalable Time-Domain CNN Accelerator with Full-Swing Delay Cell and Gray-Code TDC in 28-nm CMOS**

» Mr. Sangsu Jeong (Korea, Republic of)[1], Mr. Huiwon Yun (Korea, Republic of)[1], Mr. Dongkwon Lee (Korea, Republic of)[1], Mr. Sunwoo Lee (Korea, Republic of)[1], Mr. Minyoung Kang (Korea, Republic of)[1], Prof. Dongsuk Jeon (Korea, Republic of)[1] (1. Seoul National University)

4:50pm **11-8: (INVITED) Demonstration of Fast OTA Chirp-Based Beam Training using Analog TTD Array with Millimeter Wave Testbed for applications in Radar Systems**

» Mr. Aditya Wadaskar (United States)[1], Mr. Hesam Abbasi (United States)[2], Mr. Sreeni Poolakkal (United States)[2], Mr. Yen-Chin Wang (United States)[1], Mr. Benjamin Domae (United States)[1], Prof. Subhanshu Gupta (United States)[2], Dr. Danijela Cabric (United States)[1] (1. University of California Los Angeles, 2. Washington State University)

5:30pm **Welcome Reception & Best Paper Candidate Poster Session**

Skyline Ballroom

Tuesday, 15 April

8am **Analog Circuits and Techniques IV - Session 14: Innovations in High-Performance Analog and Mixed-Signal Circuit Design**

Grand Ballroom

Chaired by: Ping-hsuan Hsieh (Taiwan)

8am **14-1: A 106.1dB DR, 450µA Idle Current Class-H Piezoelectric MEMS Micro-Speaker Driver with Envelope Tracking, Digital and Analog Inputs and Less Than 2.1µs Latency**

» Dr. Francesco Rezzi (Italy)[1], Dr. Vittorio Colonna (Italy)[1], Dr. Gabriele Gandolfi (Italy)[1], Dr. Samuele Fusetto (Italy)[1], Dr. Michele Chiabrera (Italy)[1], Dr. Alessandro Savo (Italy)[1], Dr. Maurizio Costagliola (Italy)[1], Dr. Ruggero Stella (Italy)[1], Dr. Matteo Bulzi (Italy)[1], Dr. Sebastian Radosav (Italy)[1], Dr. Domenico Granozio (Italy)[1], Dr. Giuseppe Alfieri (Italy)[1], Dr. Alessandro Gemelli (Italy)[2], Prof. Piero Malcovati (Italy)[2], Prof. Edoardo Bonizzoni (Italy)[2] (1. Inventvm Semiconductor SRL, 2. University of Pavia)

8:25am **14-2: A -117.1dB THD Audio Decoder Utilizing Single Vector Quantizer for Simultaneous Mismatch and ISI Shaping**

» Mr. Yuxiang Tang (China)[1], Mr. Yijie Li (China)[1], Mr. Kaiwen Zhou (China)[1], Mr. Qi Luo (China)[1], Mr. Xining Zhang (China)[1], Mr. Yongda Ma (China)[1], Prof. Zhiliang Hong (China)[1], Prof. Jiawei Xu (China)[1] (1. Fudan University)

Continued from **Tuesday, 15 April**

8:50am

14-3: A 22.0-to-28.4GHz 192.2dBc/Hz FoM and 206.2dBc/Hz FoMA Dual-Core VCO Using Circular-Inverse-Class-F Topology under Standard Supply Voltage in 65nm CMOS process

» Mr. Huanyu Ge (China)[1], Prof. Haikun Jia (China)[1], Prof. Wei Deng (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

9:15am

14-4 (BEST STUDENT PAPER CANDIDATE): A Resistive Dynamic Bias Comparator with Flying Capacitors Achieving 129μVrms Input-Referred Noise at 1GS/s in 28nm FD-SOI

» Mr. Byeongjin Son (Korea, Republic of)[1], Mr. Heungsik Eum (Korea, Republic of)[1], Mr. Hyeonjun Pi (Korea, Republic of)[1], Prof. Youngcheol Chae (Korea, Republic of)[1] (1. Yonsei University)

8am

Wireless Transceivers and RF/mm-Wave Circuits and Systems III -

Session 15: Panel: mmWave/THz Design: A New Paradigm or a Repeat of History with Faster Transistors?

Olympia

Chaired by: Dr. Mark Oude Alink (Netherlands) and Prof. Taiyun Chi (United States)

8am

Power Management III -

Session 16: Application-Specific Power Management

Michelangelo

Chaired by: Sriharsh Pakala (United States) and Mauro Leoncini (Italy)

8am

16-1 (BEST STUDENT PAPER CANDIDATE): A Multi-Level Power Management Architecture for Battery-Powered SPAD Drivers with Supply Intrinsic Quenching and 10-ns Dead Time

» Mr. Wenshuo Zhu (United States)[1], Ms. Xuan Sun (United States)[1], Dr. Xin Zhang (United States)[2], Dr. Cheng Huang (United States)[1] (1. Iowa State University, 2. IBM T. J. Watson Research Center)

8:25am

16-2: A Parallel-Input Energy-Recycling Power Management Unit with Continuous MPPT for Magnetoelectrically Powered mm-Scale Bio-Implants

» Mr. Yiwei Zou (United States)[1], Mr. Huan-Cheng Liao (Taiwan)[1], Mr. Wei Wang (United States)[1], Mr. Wonjune Kim (United States)[1], Mr. Yumin Su (United States)[1], Dr. Jacob Robinson (United States)[1], Prof. Kaiyuan Yang (United States)[1] (1. Rice University)

8:50am

16-3: A 30-110V Resonant Buck-Boost Power-Bus Charger Achieving 50-A Peak Laser-Current Pulse Generation in 2ns for MHz-Frequency Automotive LiDAR Transmitter

» Mr. Hangxiao Ma (Macao)[1], Mr. Qiaobo Ma (Macao)[1], Mr. Xuchu Mu (Macao)[1], Prof. Yang Jiang (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Pui-In Mak (Macao)[1] (1. University of Macau)

9:15am

16-4: A 40.68MHz Dual-Output Wireless Power Transfer System Achieving 149.7mW Maximum Power and 90.3%/51.2% RX/E2E Efficiency with 8mm-Diameter RX Coil

» Mr. Tianqi Lu (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

8am

Systems and Security I -

Session 17: Next-Generation Systems: From Datacenters to the Edge

Aquitania

Chaired by: Monodeep Kar (United States) and Dr. Baibhab Chatterjee (United States)

8am

17-1: TD-dAJC: A 2pJ/pixel Time-Domain Weight and Integrating-MAC based direct-Analog-to-MJPEG Compression for Video Sensor Nodes

» Mr. Gourab Barik (United States)[1], Mr. Harshit Naman (United States)[1], Mr. Yudhajit Ray (United States)[1], Dr. Shreyas Sen (United States)[1] (1. Purdue University)

Continued from **Tuesday, 15 April**

8:25am

17-2 (BEST STUDENT PAPER CANDIDATE): A 28-nm Real-Time Reinforcement Learning Processor for Mapless Autonomous Navigation with Unified Actor-Critic Network and Inference-on-Request Scheduling

» Mr. Juyoung Oh (Korea, Republic of)[1], Ms. Jie-Xin Liu (Taiwan)[2], Mr. Yi-Chen Teng (Taiwan)[2], Prof. Hsueh-Cheng Wang (Taiwan)[2], Prof. Dongsuk Jeon (Korea, Republic of)[1] (1. Seoul National University, 2. National Yang Ming Chiao Tung University)

8:50am

17-3: Forward Error Correction Requirements for Data Center Connectivity

» Mr. Han-Mo Ou (United States)[1], Mr. Gene Lee (United States)[1], Prof. Naresh Shanbhag (United States)[1] (1. University of Illinois at Urbana-Champaign)

9:15am

17-4: A 0.14μJ per-Acquisition Frequency-Domain GPS Correlator Using Adaptive Compressive Sampling

» Mr. Jung-Jin Park (United States)[1], Mr. Julian Arenas (United States)[1], Mr. Kevin Patino-Sosa (United States)[1], Prof. Visvesh Sathe (United States)[1] (1. Georgia Institute of Technology)

8am

Digital Circuits and SoCs III -
Session 18: Digital Compute-in-Memory

Brittannic

Chaired by: Ashwin Lele (United States) and Ningyuan Cao (United States)

8am

18-1: A 28nm 20.9-137.2 TOPS/W Output-Stationary SRAM Compute-in-Memory Macro Featuring Dynamic Look-ahead Zero Weight Skipping and Runtime Partial Sum Quantization

» Mr. Xiaofeng Hu (United States)[1], Dr. HanGyeol Mun (United States)[1], Mr. Jian Meng (United States)[1], Mr. Yuan Liao (United States)[1], Mr. Amitesh Sridharan (United States)[2], Dr. Jae-sun Seo (United States)[1] (1. Cornell Tech, 2. Arizona State University)

8:25am

18-2: A 28nm Value-Wise Hybrid-Domain Compute-In-Memory Macro with Heterogeneous Memory Fabric and Asynchronous Sparsity Manager

» Mr. Yuanzhe Zhao (Macao)[1], Dr. Yang Wang (China)[2], Mr. Yuheng Wang (Macao)[1], Mr. Heng Xie (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. Rui P. Martins (Macao)[1], Prof. Chi-Hang Chan (Macao)[1], Prof. Shouyi Yin (China)[2], Prof. Minglei Zhang (Macao)[1] (1. University of Macau, 2. Tsinghua University)

8:50am

18-3: Pro-Cache-CIM: A 28nm 69.4TOPS/W Product-Cache-based Digital-Compute-in-Memory Macro Leveraging Data Locality Pattern in Vision AI tasks

» Mr. Wenbin Jia (China)[1], Mr. Yifan He (China)[1], Mr. Xiang Li (China)[2], Mr. Yixuan Xie (China)[1], Ms. Zongle Huang (China)[1], Mr. Wenxun Wang (China)[1], Mr. Boju Chen (China)[1], Mr. Yaolei Li (China)[1], Prof. Jinshan Yue (China)[3], Prof. Xueqing Li (China)[1], Prof. Huazhong Yang (China)[1], Prof. Hongyang Jia (China)[1], Prof. Yongpan Liu (China)[1] (1. Tsinghua University, 2. Tsinghua Shenzhen International Graduate School, 3. Institute of Microelectronics of the Chinese Academy of Sciences)

9:15am

18-4: A 52.03TOPS/W DCIM-Based Accelerator with FlashAttention and Sparsity-Aware Alignment for LLMs

» Prof. Bo Liu (China)[1], Mr. Xingyu Xu (China)[1], Mr. Yang Zhang (China)[1], Mr. Xilong Kang (China)[1], Mr. Qingwen Wei (China)[1], Mr. Zihan Zou (China)[1], Prof. Jun Yang (China)[1], Prof. Hao Cai (China)[1], Prof. Xin Si (China)[1] (1. southeast university)

9:40am

Break

Grand Ballroom Foyer

10:05am

Analog Circuits and Techniques V -
Session 19: Forum: Potential of Open Source Design for Analog/Mixed Signal IC Education

Grand Ballroom

Chaired by: Jorge Marin (Chile) and Nazanin Neshatvar (United Kingdom)

Continued from **Tuesday, 15 April**

10:05am **Emerging Technology II -**
Session 20: Panel: Wireline and Lightwave Interconnects - The Shifting Boundary in the AI Era
Olympia
Chaired by: Win-san (Vince) Khwa (Taiwan) and Henry Park

10:05am **Power Management III cont'd -**
Session 16: Application-Specific Power Management
Michelangelo
Chaired by: Sriharsh Pakala (United States) and Mauro Leoncini (Italy)

10:05am **16-5: A 93.9% Peak Efficiency 3V-to-40V-Input GaN-based DC-DC Converter with Unified Reliability and Efficiency Adaptive Control**
» Mr. Zhaoqing Wang (United States)[1], Mr. Yichen Xu (United States)[1], Dr. Suhwan Kim (United States)[2], Dr. Nachiket Desai (United States)[2], Dr. Minxiang Gong (United States)[2], Dr. Ram Krishnamurthy (United States)[2], Dr. Xin Zhang (United States)[3], Prof. Mingoo Seok (United States)[1] (1. Columbia University, 2. Intel, 3. IBM T. J. Watson Research Center)

10:30am **16-6: A Fully Integrated Adaptive-MPP-Shifting Rectifier for Piezoelectric Energy Harvesting Outputting 580μW at 10V-VOC**
» Ms. Xinling Yue (Netherlands)[1], Mr. Wenyu Peng (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

10:55am **16-7: A 0.49W 120-230VRMS to 8-12VDC Power Converter with Switched-Capacitor Regulation and Rectifier Short Flipping Achieving Maximized Bridge Conduction Time**
» Mr. Tianqi Lu (Netherlands)[1], Mr. Xianglong Li (Netherlands)[1], Mr. Wenyu Peng (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

11:20am **16-8: An 81.0% Peak Efficiency, 1.0W/cm^3 Miniaturized 5V/1A AC-DC Converter using a Highly-Integrated Primary-Side Active Clamp Flyback Controller with Adaptive Frequency and Zero-Voltage Switching**
» Mr. Akiyoshi Tanaka (United States)[1], Ms. Shan He (United States)[1], Mr. Reza Mounesi (United States)[2], Dr. Xinjian Liu (United States)[1], Mr. Omar Faruqe (United States)[1], Ms. Nugaira Gahan Mim (United States)[1], Dr. Daniel Truesdell (United States)[1], Prof. Adel Nasiri (United States)[2], Prof. Benton Calhoun (United States)[1] (1. University of Virginia, 2. University of South Carolina)

10:05am **Digital Circuits and SoCs III cont'd -**
Session 18: Digital Compute-in-Memory
Brittannic
Chaired by: Ashwin Lele (United States) and Ningyuan Cao (United States)

10:05am **18-5: A 22nm 29.3TOPS/W End-to-End CIM-Utilization-Aware Accelerator with Reconfigurable 4D-CIM Mapping and Adaptive Feature Reuse for Diverse CNNs and Transformers**
» Ms. Jin Wang (China)[1], Mr. Moxiao Lou (China)[1], Mr. Zhengke Yang (China)[1], Mr. Ruijie Peng (China)[1], Mr. Humiao Li (China)[1], Mr. Weirong Dong (China)[1], Mr. Haoran Lyu (China)[1], Mr. Yida Li (China)[1], Prof. Jiamin Li (China)[1], Prof. Hao Yu (China)[1], Prof. Jerald Yoo (Korea, Republic of)[2], Prof. Longyang Lin (China)[1] (1. Southern University of Science and Technology, 2. Seoul National University)

10:30am **18-6: A One-Shot Floating-Point Compute-in-Memory Macro Featuring PVT Robustness and Mismatch Tolerance for Edge LLMs**
» Mr. Yuanzhe Zhao (Macao)[1], Mr. Heng Xie (Macao)[1], Mr. Zijian Wang (Macao)[1], Mr. Chunlin Tian (Macao)[1], Prof. Li Li (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Chi-Hang Chan (Macao)[1], Prof. Minglei Zhang (Macao)[1] (1. University of Macau)

10:55am **18-7: (INVITED) Tracking Fmax Degradation of a RISC-V CPU with Synthesizable Odometer Aging Sensors**
» Ms. Tahmida Islam (United States)[1], Mr. Junkyu Kim (United States)[1], Mr. Hanzhao Yu (United States)[1], Prof. Chris Kim (United States)[1] (1. University of Minnesota)

12pm **Session 21: Keynote Luncheon**
Skyline Ballroom

Continued from **Tuesday, 15 April**

12pm

Circuit Labs at the Lunch Table with MOSbius

» Prof. Peter Kinget (United States)[1] (1. Bernard J. Lechner Professor of Electrical Engineering, Columbia University)

1:30pm

Wireless Transceivers and RF/mm-Wave Circuits and Systems IV - Session 22: High Performance Transceivers

Grand Ballroom

Chaired by: Mustafijur Rahman (India) and Prof. Vadim Issakov (Germany)

1:30pm

22-1: A CMOS 228-324GHz RF Domain Quadrature Receiver with a Broadband Harmonic-Enhanced LO Generator

» Prof. Weiping Wu (China)[1], Ms. Xun Bao (China)[1], Mr. Shi Chen (China)[1], Mr. Jingze Wang (China)[1], Ms. Shulan Chen (China)[1], Prof. Yan Wang (China)[1], Prof. Lei Zhang (China)[1] (1. School of Integrated Circuits， Tsinghua University)

1:55pm

22-2: A 22-to-32 GHz 4-Beam 32-Element Polarization Reconfigurable Fully-Connected Fully-Bidirectional MIMO Transceiver for Emerging Space-air-ground-sea Integrated Network

» Mr. Junlong Gong (China)[1], Prof. Wei Deng (China)[1], Mr. Shulin Yao (China)[1], Prof. Haikun Jia (China)[1], Ms. Xinyu Jiang (China)[1], Mr. Xiangyu Nie (China)[1], Ms. Dongfang Li (China)[1], Mr. Hongliang Wu (China)[1], Dr. Chuanming Zhu (China)[1], Dr. Xiangrong Huang (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

2:20pm

22-3: A 6-18-GHz Reflectionless Blocker-canceling Mixer-first Receiver with Maximum 55.6-dB Out-of-band Rejection for Satellite Communication Systems

» Mr. Kai Li (China)[1], Mr. Jialei Wu (China)[1], Prof. Keping Wang (China)[1] (1. Tianjin University)

2:45pm

22-4: A Compact Reconfigurable 24-29.5/38-43.5GHz Phased Array Transceiver Front-End with Self-Interference Rejection and Wideband IF Supporting TDD/FDD Operation

» Mr. Qin Chen (China)[1], Mr. Xuhao Jiang (China)[1], Mr. Xuanxuan Yang (China)[2], Mr. Yuchen Liang (China)[2], Mr. Ziang Zhang (China)[2], Mr. Junbo Liu (China)[2], Mr. Yifei Hu (China)[2], Dr. Depeng Cheng (China)[3], Dr. Long He (China)[3], Prof. Xu Wu (China)[1], Prof. Lianming Li (China)[1] (1. Southeast University, Purple Mountain Laboratories, 2. southeast university, 3. Purple Mountain Laboratories)

1:30pm

Emerging Technology III - Session 23: Cryogenic and Silicon Photonic ICs

Olympia

Chaired by: Andrea Ruffino (Switzerland) and Juhwan Yoo (United States)

1:30pm

23-1: (INVITED) Integrated photonic-electronic deep neural networks: from sub-nanosecond image classification to PVT-tolerant activation functions

» Mr. Amirreza Shoobi (United States)[1], Mr. Alexander Geers (United States)[1], Mr. Anish Mondal (United States)[1], Dr. Kaisarbek Omirzakhov (United States)[1], Dr. Farshid Ashtiani (United States)[1], Prof. Firooz Aflatouni (United States)[1] (1. University of Pennsylvania)

2:20pm

23-2: A 4.6-373K Functional 800MS/s 12b Buffer-then-Amplify Charge-Pump-Based Pipelined TI-SAR ADC with Integrated-Active-Hold Technique

» Mr. Kaoru Yamashita (Japan)[1], Prof. Kentaro Yoshioka (Japan)[2], Mr. Christian Ziegler (Germany)[1], Prof. Vadim Issakov (Germany)[1], Prof. Hiroki Ishikuro (Japan)[2] (1. Technical University of Braunschweig, 2. Keio University)

2:45pm

23-3: A PMOS-Based Deep Cryogenic CMOS Temperature Sensor Achieving a Range from 10K to 410K with a Relative Inaccuracy of 0.5% (3σ)

» Mr. Xingyu Qi (China)[1], Mr. Yingzhe Sha (China)[1], Prof. Xufeng Kou (China)[2], Prof. Xiaoyong Xue (China)[1], Prof. Peng Wang (China)[3], Prof. Zhangcheng Huang (China)[1], Prof. Qi Liu (China)[1], Prof. Ming Liu (China)[1] (1. Fudan University, 2. Shanghaitech University, Shanghai, China, 3. Shanghai Institute of Technical Physics, Chinese Academy of Sciences)

Continued from **Tuesday, 15 April**

1:30pm **Power Management IV - Session 24: Hybrid DC-DC Converters**

Michelangelo

Chaired by: Prof. Mo Huang (Macao) and Dr. Suhwan Kim (United States)

1:30pm **24-1: (INVITED) Where is the Inductor: A Review and Comparison of the Hybrid DC-DC Buck Topologies**

» Dr. Zhiguo Tong (Macao)[1], Mr. Wenjie Yang (Macao)[2], Dr. Shousheng Han (China)[1], Dr. Junwei Huang (Macao)[2], Dr. Xiangyu Mao (Macao)[2], Prof. Yan Lu (China)[3] (1. Tsinghua University and University of Macau, 2. University of Macau, 3. Tsinghua University)

2:20pm **24-2: A 94.5%-Peak-Efficiency Dual-Path Single-Inductor Dual-Output Converter with Reduced Inductor Current and Output Voltage Ripple**

» Mr. Baochuang Wang (China)[1], Prof. Lin Cheng (China)[1] (1. University of Science and Technology of China)

2:45pm **24-3: A 100A 48-60V to 1V Hybrid LLC Resonant Converter with 51mV Droop for a 70A/20ns Load Transient**

» Mr. Zeguo Liu (China)[1], Mr. Zhiren Luo (China)[1], Mr. Xiangan You (China)[2], Mr. Dongjie Ye (China)[1], Mr. Weiyi Tang (China)[1], Mr. Qinyang Wang (China)[1], Dr. Qidong Wang (China)[2], Dr. Jianliang Shen (China)[3], Prof. Lin Cheng (China)[1] (1. University of Science and Technology of China, 2. Institute of Microelectronics of the Chinese Academy of Sciences, 3. Information Engineering University)

1:30pm **Wireline and Optical Communications Circuits and Systems I - Session 25: High-speed Wireline and Optical Communication**

Aquitania

Chaired by: Shenggao (Victor) Li (United States) and Luca Ravezzi (United States)

1:30pm **25-1: (INVITED) A 224Gb/s 3pJ/bit 42dB Insertion Loss Post-FEC Error Free Transceiver in 3-nm FinFET CMOS**

» Dr. Dirk Pfaff (Canada)[1], Dr. Muhammad Nummer (Canada)[1], Dr. Noman Hai (Canada)[1], Dr. Jingjing Xia (Canada)[1], Mr. Kai Ge Yang (Canada)[1], Mr. Mohammad-Mahdi Mohsenpour (Canada)[1], Mr. Choon-Haw CH Leong (Canada)[1], Dr. Marc-Andre LaCroix (Canada)[1], Mr. Babak Zamanlooy (Canada)[1], Mr. Tom Eeckelaert (Canada)[1], Mr. Dmitry Petrov (Canada)[1], Mr. Mostafa Haroun (Canada)[1], Mr. Carson Dick (Canada)[1], Mr. Alif Zaman (Canada)[1], Mr. Haitao Mei (Canada)[1], Dr. Tahseen Shakir (Canada)[1], Mr. Carlos Carvalho (Canada)[1], Mr. Howard Huang (Canada)[1], Mr. Ralph Mason (Canada)[1], Mrs. Fahmida Brishty (Canada)[1], Mrs. Ifrah Jaffri (Canada)[1], Mr. David Yokoyama-Martin (Canada)[1] (1. Synopsys, Inc.)

2:20pm **25-2: An 800GbE PAM-4 PHY transceiver that supports 42dB copper and direct-drive optical applications in 7nm**

» Mr. Chang Liu (United States)[1], Dr. Burak Catli (United States)[1], Dr. Yong Liu (United States)[1], Mr. Anand Vasani (United States)[1], Dr. Guansheng Li (United States)[1], Mr. Kun Chuai (United States)[1], Dr. Lakshmi Rao (United States)[1], Mr. Yang Liu (United States)[1], Dr. Xin Meng (United States)[1], Mr. Jiawen Zhang (United States)[1], Mr. Tim He (United States)[1], Dr. Batu Dayanik (United States)[1], Dr. Vadim Milirud (United States)[1], Dr. Meisam Honarvar Nazari (United States)[1], Dr. Hyo Gyuem Rhew (United States)[2], Dr. Derui Kong (United States)[1], Mr. Arvindh Iyer (United States)[1], Mr. Nan Wang (United States)[1], Dr. Alireza Nilchi (United States)[1], Dr. Aminghasem Safarian (United States)[1], Dr. Ray Wang (United States)[1], Dr. Hyung-Joon Jeon (United States)[1], Dr. Xiaochen Yang (United States)[1], Dr. Boyu Hu (United States)[1], Dr. Jerry Han (United States)[1], Mr. Adesh Garg (United States)[1], Mr. Kumar Thasari (United States)[1], Dr. Heng Zhang (United States)[1], Dr. Namik Kocaman (United States)[1], Mr. Ali Nazemi (United States)[1], Dr. Delong Cui (United States)[1], Dr. Afshin Momtaz (United States)[1], Dr. Jun Cao (United States)[1] (1. Broadcom Inc, 2. now with Samsung Electronics)

2:45pm **25-3: A 100Gb/s Transmitter with Digital Pre-Distortion and MUX-Merged Voltage-Mode Driver Achieving 3-times INLPP Improvement in 28-nm CMOS**

» Mr. Chenxi Han (China)[1], Dr. Xiaoteng Zhao (China)[1], Mr. Qi Zhang (China)[1], Dr. Yuan Liu (China)[1], Mr. Yuhao Zhang (China)[1], Dr. Hongzhi Liang (China)[1], Dr. Yukui Yu (China)[1], Prof. Shubin Liu (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

Continued from **Tuesday, 15 April**

1:30pm **Biomedical Technologies and Applications I -**
Session 26: Advanced Biopotential Interfaces
Brittannic
Chaired by: Sahil Shah (United States) and Prof. Youngcheol Chae (Korea, Republic of) and Shih-Chii Liu (Switzerland)

1:30pm **26-1: (INVITED) In-Ear EEG Auditory Neurofeedback Towards Unobtrusive Sleep Enhancement**
» Mr. Min Suk Lee (United States)[1], Mr. Zhaoyi Liu (United States)[1], Mr. Abhinav Uppal (United States)[1], Dr. Jiahao Song (United States)[2], Dr. Akshay Paul (United States)[2], Dr. Florian Chapotot (United States)[3], Dr. Esra Tasali (United States)[3], Dr. Yuchen Xu (United States)[2], Prof. Gert Cauwenberghs (United States)[1] (1. University of California San Diego, 2. Institute for Neural Computation, 3. University of Chicago)

2:20pm **26-2 (BEST STUDENT PAPER CANDIDATE): A 32-channel 85.4dB SNDR Time-multiplexed Neural Recording Front-end Achieving within-conversion Artifact Recovery**
» Mr. Arindam Mandal (United States)[1], Dr. Chi-Hsiang Huang (United States)[1], Mr. Julian Arenas (United States)[1], Mr. Wei-En Lee (United States)[1], Mr. Philip Anschutz (United States)[1], Dr. Amanda Jacob (United States)[2], Dr. Keshav Ramachandra (United States)[2], Prof. Samuel Sober (United States)[2], Prof. Muhannad Bakir (United States)[1], Prof. Shaolan Li (United States)[1], Prof. Visvesh Sathe (United States)[1] (1. Georgia Institute of Technology, 2. Emory University)

2:45pm **26-3: An Implantable Fully-Packaged Current-Controlled Wireless Near-Adiabatic Neural Stimulator Achieving 71.7% Peak Efficiency and 13.5% Efficiency Variation Across Supported Stimulation Current Range**
» Mr. Hong Liao (China)[1], Mr. Wentao Ma (China)[1], Ms. Xiaoxu Yang (China)[1], Ms. Jianfang Nie (China)[1], Ms. Bingfang Wang (China)[1], Mr. Zhiqiang Chang (China)[1], Prof. Yin Fang (China)[1], Prof. Jiangfeng Wu (China)[1], Prof. Miao Meng (China)[1] (1. Tongji University)

3:10pm **Break**
Grand Ballroom Foyer

3:35pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems IV cont'd -**
Session 22: High Performance Transceivers
Grand Ballroom
Chaired by: Prof. Vadim Issakov (Germany) and Mustafijur Rahman (India)

3:35pm **22-5: A 0.9mm2 SDR Receiver in 40-nm CMOS Covering 10-72GHz Using Inductor-Less Edge-combining based LO Quintupler**
» Mr. Haoyu Bai (China)[1], Ms. Ling Hao (China)[1], Dr. Dong Wang (China)[1], Ms. Keer Gao (China)[1], Mr. Han Huang (China)[1], Mr. Jiazheng Zhou (China)[1], Mr. Jiaqi He (China)[1], Prof. Junhua Liu (China)[1], Prof. Huailin Liao (China)[1] (1. Peking University)

4pm **22-6: A Packaged D-band Transmitter with a Multifeed Lens Antenna Achieving 25.3dBm Single-element EIRP for 2-D Scalable Arrays**
» Mr. Hang Wang (United States)[1], Dr. Hao Guo (United States)[1], Dr. Xiaohan Zhang (United States)[1], Dr. Taiyun Chi (United States)[1] (1. Rice University)

4:25pm **22-7: A 14.08-Gb/s 256-QAM 60GHz Phased-Array Transceiver with Switchable Tertiary-Coil Transformer T/R Switch and Customizable-Sized Cascade Phase-Invariant VGAs**
» Mr. Xuwei Li (China)[1], Dr. Depeng Cheng (China)[2], Mr. Jing Feng (China)[1], Mr. Xin Chen (China)[1], Mr. Rui Cao (China)[1], Mr. Lei Luo (China)[1], Mr. Haipeng Duan (China)[1], Prof. Dongming Wang (China)[3], Prof. Lianming Li (China)[3] (1. southeast university, 2. Purple Mountain Laboratories, 3. Southeast University, Purple Mountain Laboratories)

4:50pm **22-8: A 27-39GHz 48Gbit/s 8-Channel Phased Array Transceiver Frontend with Broadband TX/RX Co-Design Optimization**
» Mr. Niccolò Villaggi (Switzerland)[1], Mr. Yuqi Liu (Switzerland)[1], Dr. Tzu-Yuan Huang (Switzerland)[1], Prof. Sensen Li (United States)[2], Prof. Taiyun Chi (United States)[3], Prof. Hua Wang (Switzerland)[1] (1. ETH Zurich, 2. The University of Texas at Austin, 3. Rice University)

Continued from **Tuesday, 15 April**

3:35pm **Emerging Technology IV -**
Session 27: Forum: Probabilistic Computing
Olympia
Chaired by: Tathagata Srimani (United States) and Win-san (Vince) Khwa (Taiwan)

3:35pm **Power Management IV cont'd -**
Session 24: Hybrid DC-DC Converters
Michelangelo
Chaired by: Prof. Mo Huang (Macao) and Dr. Suhwan Kim (United States)

3:35pm **24-4: A 1.8V Input, 96.5% Efficiency, 4.05A/mm2 FoM, Three-Level Dual-Path Hybrid Buck Converter with Mitigated Capacitive Inrush Current and Seamless DVS Across a Wide 0.4-to-1.5V Output Range**
» Mr. Jae-Hyun Kim (Korea, Republic of)[1], Mr. Jun-Gi Lee (Korea, Republic of)[1], Dr. Hyunki Han (Korea, Republic of)[1], Prof. Hyun-Sik Kim (Korea, Republic of)[1] (1. KAIST)

4pm **24-5: An Inductor-First Hybrid Buck-Boost Converter Featuring Seamless Single-Mode Operation, 97.2% Peak Efficiency, and 565mA/mm3 Current Density with Ultra-Compact 1mm3-Volume Inductor**
» Mr. Hyunjun Park (Korea, Republic of)[1], Mr. Yunho Lee (Korea, Republic of)[1], Mr. Minsu Kim (Korea, Republic of)[1], Dr. Woojoong Jung (Korea, Republic of)[1], Mr. Hongseok Kim (Korea, Republic of)[1], Prof. Hyung-Min Lee (Korea, Republic of)[1] (1. Korea University)

4:25pm **24-6: A 98.5% Peak Efficiency 2/3-Phase Buck-or-Boost Converter With VCR-Independent Loss Optimization and Unconditional RHP Zero Elimination Achieving 2.76A/mm2-Current-Density and 6.5µs Recovery**
» Mr. Xiongjie Zhang (Macao)[1], Ms. Xinman Li (Macao)[1], Prof. Yang Jiang (Macao)[1], Prof. Zhangming Zhu (China)[2], Prof. Rui P. Martins (China)[1], Prof. Pui-In Mak (Macao)[1] (1. University of Macau, 2. Xidian University)

4:50pm **24-7: A 12V/24V-to-1V Shared Switched-Capacitor Multi-Inductor Multi-Output Converter with 90.9%/89.5% Peak Efficiency and Negligible Cross Regulation**
» Ms. Yiling Xie (China)[1], Prof. Jianping Guo (China)[1] (1. Sun Yat-sen University)

3:35pm **Wireline and Optical Communications Circuits and Systems I cont'd -**

Session 25: High-speed Wireline and Optical Communication
Aquitania
Chaired by: Shenggao (Victor) Li (United States) and Luca Ravezzi (United States)

3:35pm **25-4 (BEST REGULAR PAPER CANDIDATE): BASS-PLL: A Bandwidth Augmented Sub-Sampling PLL Achieving a Wide Bandwidth Above 30% of the Reference Frequency and a Worst Case FoMREF of -247.9dB at 3GHz with a Ring Oscillator**
» Ms. xueke cai (China)[1], Ms. Tong Zhang (China)[1], Mr. Weihao Jie (China)[1], Ms. Yanling Zheng (China)[1], Mr. Deyong Li (China)[1], Ms. Yiwen Zhang (China)[1], Mr. Yang Zhao (China)[1], Prof. Yongfu Li (China)[1], Prof. Honglan Jiang (China)[1], Prof. Patrick Mercier (United States)[2], Prof. Hui Wang (China)[1] (1. Shanghai Jiao Tong University, 2. University of California San Diego)

4pm **25-5: A 0.3-to-10.1GHz 33.8fsRMS-Jitter Hybrid Injection-Locked Eight-Phase Clock Generator with Adaptive Mismatch Cancellation Technique for High-Speed Links in 28nm CMOS**
» Mr. Hongzhi Wu (China)[1], Mr. Xuxu Cheng (China)[1], Mr. Liping Zhong (China)[1], Mr. Yangyi Zhang (China)[1], Mr. Weitao Wu (China)[1], Mr. Xiongshi Luo (China)[1], Prof. Alex Pan (China)[1] (1. Southern University of Science and Technology)

4:25pm **25-6: A DAC-based Transmitter with VCSEL Bias-Current Generation enabling 180 Gbit/s PAM-8 Electrical and 100 Gbit/s PAM-4 VCSEL-based Transmission in 22nm SOI**
» Mr. Urs Hecht (Germany)[1], Dr. Philipp Scholz (Germany)[1], Mr. Patrick Kurth (Germany)[1], Mr. Frowin Buballa (Germany)[1], Ms. Helia Ordouei (Germany)[1], Prof. Friedel Gerfers (Germany)[1] (1. Technische Universität Berlin)

Continued from **Tuesday, 15 April**

4:50pm

25-7: A CMOS Low-Noise BM-TIA Employing Current Injection Accelerator for 50G-PON with CM-Post-Amplifier Chip Connectivity

» Mr. Yifei Xia (China)[1], Mr. Zhixing Zhang (China)[1], Mr. Shuaizhe Ma (China)[1], Mr. Yuanhao Yao (China)[1], Mr. Ruixuan Yang (China)[1], Ms. Yuye Yang (China)[1], Mr. Jianyu Yang (China)[1], Prof. Li Geng (China)[1], Prof. Dan Li (China)[1] (1. Xi'an Jiaotong University)

3:35pm

Biomedical Technologies and Applications I cont'd - Session 26: Advanced Biopotential Interfaces

Brittannic

Chaired by: Sahil Shah (United States) and Prof. Youngcheol Chae (Korea, Republic of) and Shih-Chii Liu (Switzerland)

3:35pm

26-4: A 6μW ECG-Recording ΔΣ Modulator with Internal-Capacitor-Flipping Technique for 34Vpp Common-Mode-Interference (CMI) Tolerance and 1Vpp Input Range

» Ms. Jimin Koo (Korea, Republic of)[1], Mr. Sein Oh (Korea, Republic of)[1], Dr. Yoontae Jung (Belgium)[2], Mr. Vincent Lukito (Korea, Republic of)[1], Prof. Sohmyung Ha (United Arab Emirates)[3], Prof. Minkyu Je (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology, 2. IMEC, 3. New York University Abu Dhabi)

4pm

26-5: A Tripolar Stimulator with Return-Electrode-Based Charge-Pack Injection Technique for Charge Imbalance Correction in Spatiotemporal Stimulation

» Mr. Jialei Wu (China)[1], Ms. Simeng Yin (China)[1], Mr. Yixin Zhou (China)[2], Mr. Jianye Li (China)[1], Mr. Kai Li (China)[1], Prof. Xiaoyan Shen (China)[3], Ms. Tinghui Sun (China)[3], Mr. Xinlong Zhang (China)[3], Prof. Keping Wang (China)[1] (1. Tianjin University, 2. southeast university, 3. Nantong University)

4:25pm

26-6: An 81.7MΩ-Input-Impedance 179.5dB-FOMSNDR 1.8VPP-Input-Range Noise-Shaping-SAR-Based Sensing Frontend with Dynamic Input-Impedance Boosting and Prediction-Assisted Mismatch-Shaping-DEM

» Mr. Yiming Han (United States)[1], Dr. Linran Zhao (United States)[1], Mr. Tzuping Huang (United States)[1], Dr. Alper Bozkurt (United States)[2], Dr. Yaoyao Jia (United States)[1] (1. The University of Texas at Austin, 2. North Carolina State University)

4:50pm

26-7: A Scalable 256-Channel 12-mA 0.06%-Current-Mismatch 22-V Neurostimulator with Real-time Current Calibration and Compliance Monitoring

» Mr. Po-Han Chen (United States)[1], Mr. Zhiheng Luo (United States)[1], Mr. Spencer Chang (United States)[1], Mr. Kristopher Ngo (United States)[1], Mr. Ritwik Vatsyayan (United States)[1], Mr. Jihwan Lee (United States)[1], Ms. Tara S. Porter (United States)[1], Prof. Drew A. Hall (United States)[1], Prof. Shadi Dayeh (United States)[1], Prof. Ian Galton (United States)[1], Prof. Hanh-Phuc Le (United States)[1] (1. University of California San Diego)

5:30pm

IEEE SSCS Young Professionals and Women in Circuits Mentoring Event

Michelangelo

6pm

CICC Conference Reception & Industry Information Session

Skyline Ballroom

Wednesday, 16 April

8:30am

Welcome

Grand Ballroom

8:50am

Keynote Session

Grand Ballroom

Continued from **Wednesday, 16 April**

8:50am

The role of Intelligent Memory in enabling the emergent era of Artificial Generalized Intelligence

» Dr. Samir Mittal (United States)[1] (1. CVP of AI in Silicon Systems Design of Micron)

9:40am **Break**

Grand Ballroom Foyer

10:05am **Systems and Security II -**

Session 28: Next-Generation Systems: Hardware for Quantum and Secure Computing

Grand Ballroom

Chaired by: Monodeep Kar (United States) and Dr. Baibhab Chatterjee (United States)

10:05am

28-1: (INVITED) Cryogenic CMOS circuits for future scaled quantum computing systems: challenges and solutions

» Dr. Bodhisatwa Sadhu (United States)[1], Dr. Kevin Tien (United States)[1], Dr. Sudipto Chakraborty (United States)[1], Dr. David Frank (United States)[1], Dr. Pat Rosno (United States)[2], Dr. Daniel Moertl (United States)[2], Dr. Mark Yeck (United States)[1], Dr. John Bulzacchelli (United States)[1], Dr. Daniil Frolov (United States)[1], Dr. Devin Underwood (United States)[1], Dr. Ken Inoue (United States)[2], Dr. Christian Baks (United States)[1], Dr. Daniel Ramirez (United States)[2], Dr. Jeremy Ekman (United States)[2], Dr. Ryan Black (United States)[2], Dr. Tim Schmerbeck (United States)[2], Dr. Ray Richetta (United States)[2], Dr. Dereje Yilma (United States)[2], Dr. Andrew Davies (United States)[2], Dr. Joseph Glick (United States)[1], Dr. Dorothy Wisnieff (United States)[1], Dr. Bryce Snell (United States)[2], Dr. John Timmerwilke (United States)[1], Dr. Raphael Robertazzi (United States)[1], Dr. George Zettles (United States)[2], Dr. Scott Lekuch (United States)[1], Dr. Scott Willenborg (United States)[2], Dr. Brian Gaucher (United States)[1], Dr. Daniel Friedman (United States)[1] (1. IBM T. J. Watson Research Center, 2. IBM Systems)

10:55am

28-2: High-Entropy Analog-Based Strong PUF reaching 166 F2/bit Area-to-Entropy-ratio

» Dr. Alessandro Catania (Italy)[1], Dr. Sebastiano Strangio (Italy)[1], Dr. Maksym Paliy (Italy)[1], Mr. Christian Sbrana (Italy)[2], Mr. Michele Bertozzi (Italy)[2], Prof. Giuseppe Iannaccone (Italy)[1] (1. Department of Information Engineering, University of Pisa, 2. Quantavis s.r.l., 56126, Pisa)

11:20am

28-3: A 2455µm2 1.7Gbps Side-Channel Attack-Resistant Masked HMAC-SHA256 Accelerator in Intel 4 CMOS

» Dr. Sachin Taneja (United States)[1], Dr. Vikram Suresh (United States)[1], Dr. Raghavan Kumar (United States)[1], Dr. Vivek De (United States)[1], Dr. Sanu Mathew (United States)[1] (1. Intel Corporation)

11:45am

28-4: A 54µW Design-Agnostic Clock, Voltage, and EM-Pulse Fault-Injection Attack Detection using Time-to-Voltage Conversion

» Mr. Yudhajit Ray (United States)[1], Dr. Archisman Ghosh (United States)[1], Mr. Sarthak Antal (United States)[1], Dr. Shreyas Sen (United States)[1] (1. Purdue University)

10:05am **Wireless Transceivers and RF/mm-Wave Circuits and Systems V -**

Session 29: Forum: Emerging Techniques for Phase Locked Loops

Olympia

Chaired by: Somnath Kundu (United States) and Sachin Kalia (United States)

10:05am **Data Converters III -**

Session 30: Continuous-Time ADCs

Michelangelo

Chaired by: Chia-Hung Chen (Taiwan) and Jin-tae Kim (Korea, Republic of)

10:05am

30-1 (BEST INVITED PAPER CANDIDATE): Continuous-Time Delta-Sigma Modulator with SAR-Assisted Digital Noise Coupling

» Dr. Kent Edrian Lozada (Korea, Republic of)[1], Dr. Ye-Dam Kim (Korea, Republic of)[2], Dr. Il-Hoon Jang (Korea, Republic of)[2], Prof. Seung-Tak Ryu (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology, 2. Samsung Electronics)

Continued from **Wednesday, 16 April**

10:55am **30-2: A 0.16mm2 450MHz-BW 72dB-SNDR Continuous-time Pipeline ADC with APF+HPF and APF+FIR Hybrid Delay Alignment Techniques**

» Mr. Heyang Zhao (China)[1], Mr. Yuxuan He (China)[1], Mr. Yunsong Tao (China)[1], Mr. Zhishuai Zhang (China)[1], Prof. Yong Chen (China)[1], Prof. Yi Zhong (China)[1], Prof. Lu Jie (China)[1], Prof. Nan Sun (China)[1] (1. Tsinghua University)

11:20am **30-3: A Calibration-free 80MHz CT DSM using Dual Quantization and ISI Shuffler achieving 106.2dB SFDR**

» Mr. Ahmed Abdelaal (Germany)[1], Dr. John Kauffman (Germany)[1], Dr. Joachim Becker (Germany)[1], Mr. Matteo Dalla Longa (Austria)[2], Dr. Francesco Conzatti (Austria)[2], Prof. Maurits Ortmanns (Germany)[1] (1. University of Ulm, 2. Infineon Technologies)

11:45am **30-4: A Power-Efficient Jitter-Insensitive 3.2GHz 1-bit CT ΔΣ ADC with Direct Charge Dump Feedback**

» Dr. Yanquan Luo (China)[1], Prof. Lu Jie (China)[1], Prof. Nan Sun (China)[1] (1. Tsinghua University)

10:05am **Wireline and Optical Communications Circuits and Systems II - Session 31: Energy Efficient Wireline Interconnects**

Aquitania

Chaired by: Xi Chen (United States) and Prof. Alex Pan (China)

10:05am **31-1: A 16nm 140-fJ/b/dB Dual-Mode ENRZ/NRZ Serial Data Transceiver with Dynamic Voltage Scaling**

» Dr. Armin Tajalli (Switzerland)[1], Dr. Cosimo Aprile (Switzerland)[1], Dr. Milad Ataei (Switzerland)[1], Mr. Rolf Beerwerthe (Germany)[1], Mr. Dario Carneli (Switzerland)[1], Mr. Maik Fuhs (Germany)[1], Dr. Kiarash Gharibdoust (Switzerland)[1], Dr. Ali Hormati (Switzerland)[1], Mr. James Hudner (Switzerland)[1], Mr. Victor Perrin (Switzerland)[1], Prof. Amin Shokrollahi (Switzerland)[1], Mr. Richard Simpson (Switzerland)[1], Mr. Andrew Stewart (United Kingdom)[1], Mr. David Stauffer (United States)[1], Mr. Giuseppe Surace (United Kingdom)[1], Mr. Roger Ulrich (Switzerland)[1], Mr. Mark Venneborger (Germany)[1], Mr. Patrick Urban (Germany)[1], Mr. Anant Singh (United Kingdom)[1] (1. Kandou Bus)

10:30am **31-2: A 3ns Idle-Exit Latency 0.28-28Gb/s/pin Single-Ended NRZ Die-to-Die Interface with Energy-Efficient Receiver and Background Noise Compensation**

» Mr. Hyun-Seok Choi (Korea, Republic of)[1], Mr. Sunki Cho (Korea, Republic of)[1], Dr. Sanghee Lee (Korea, Republic of)[2], Ms. Hyeri Roh (Korea, Republic of)[1], Ms. Jeong-Eun Song (Korea, Republic of)[1], Mr. Honggyoo Ahn (Korea, Republic of)[2], Ms. Jihee Kim (Korea, Republic of)[1], Mr. Minchang Kim (Korea, Republic of)[2], Dr. Hankyu Chi (Korea, Republic of)[2], Prof. Deog-Kyoon Jeong (Korea, Republic of)[1], Prof. Woo-Seok Choi (Korea, Republic of)[1] (1. Seoul National University, Seoul, Korea, 2. SK Hynix)

10:55am **31-3: An Energy and Area-Efficient PAM-4 Data Coding Scheme with Embedded Supply Noise Stabilization for Single-Ended Memory Interface**

» Mr. Giyeong Heo (Korea, Republic of)[1], Mr. Younghwan Chang (Korea, Republic of)[2], Prof. Yong-un Jeong (Korea, Republic of)[3], Dr. Jaekwang Yun (Korea, Republic of)[4], Mr. Jusung Lee (Korea, Republic of)[5], Mr. Shin-Hyun Jeong (Korea, Republic of)[1], Mr. Sanghyuk Seo (Korea, Republic of)[1], Prof. Suhwan Kim (Korea, Republic of)[1] (1. Seoul National University, Seoul, Korea, 2. S.LSI Business Division, Samsung Electronics, Korea, 3. Sejong University, 4. SK Hynix, 5. Samsung Electronics)

11:20am **31-4 (BEST STUDENT PAPER CANDIDATE): A 0.055pJ/bit/dB 42Gb/s PAM-4 Wireline Transceiver with Consecutive Symbol to Center (CSC) Encoding and Classification for 26dB Loss in 16nm FinFET**

» Mr. Ramin Javadi (United States)[1], Prof. Tejasvi Anand (United States)[1] (1. Oregon State University)

10:05am **Digital Circuits and SoCs IV - Session 32: Panel: The Impact of AI: A Job Creator or Destroyer?**

Brittannic

Chaired by: Shanshan Xie (United States) and Ashwin Lele (United States)

12pm **Lunch (on own)**

Continued from **Wednesday, 16 April**

1:30pm **Systems and Security III -**
Session 33: Advancing System Designs with Chiplet Technology (CICC/CHISIC)
Grand Ballroom
Chaired by: Richard Dorrance (United States) and Mingu Kang (United States)

1:30pm **33-1: (BEST INVITED PAPER CANDIDATE): UCIe-Compliant Chiplet Interconnect Design Leveraging Cutting-Edge Packaging Technologies**
» Mr. Yu-Jie Huang (Taiwan)[1], Mr. Mu-Shan Lin (Taiwan)[1], Mr. Chien-Chun Tsai (Taiwan)[1], Mr. Wei-Chih Chen (Taiwan)[1], Mr. Hsin-Hung Kuo (Taiwan)[1], Ms. Shu-Chun Yang (Taiwan)[1], Dr. Shenggao Li (United States)[1] (1. tsmc)

2:20pm **33-2 (BEST INVITED PAPER CANDIDATE): A high-performance Passive Base System for distributed AI/Media acceleration**
» Dr. Ragh Kuttappa (United States)[1], Mr. Jainaveen Sundaram Priya (United States)[1], Dr. Srivatsa rangachar Srinivasa (United States)[1], Mr. Paolo Aseron (United States)[2], Dr. Gauthaman Murali (United States)[1], Dr. Vinayak Honkote (United States)[1], Dr. Prerna Budhkar (United States)[1], Mr. Dileep Kurian (United States)[1], Mr. Ronald Kalim (United States)[1], Mr. Thomas P Thomas (United States)[1], Ms. Anuradha Srinivasan (United States)[1], Dr. Tanay Karnik (United States)[1] (1. Intel Corp, 2. Intel)

1:30pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems VI -**
Session 34: Design Techniques for RF/mmWave CMOS Phased-Locked Loops
Olympia
Chaired by: Hsieh-Hung Hsieh (Taiwan) and Aravind Nagulu (United States)

1:30pm **34-1: A Fractional-N Cascaded PLL Employing the Calibration-free Noise-and-Spur Cancellation technique**
» Mr. Yongqi Hu (China)[1], Mr. Jue Huang (China)[1], Mr. Chenkang Ning (China)[1], Mr. Yumeng Yuan (China)[1], Prof. Hao Xu (China)[2], Prof. Na Yan (China)[2], Prof. Xufeng Kou (China)[3] (1. Shanghaitech University, 2. Fudan University, 3. Shanghaitech University, Shanghai, China)

1:55pm **34-2: A 37.5fs-rms Jitter and -254.1dB FoM Fractional-N Sampling PLL with Reference-Phase-Selection and Complementary-DTC achieving 8x DTC Range Reduction and Zero DTC Delay Offset**
» Mr. Yanchao Liu (China)[1], Mr. Kaihang Wang (China)[1], Mr. Yang Li (China)[1], Ms. Yuchen Liu (China)[1], Dr. Xiaohua Yu (China)[1], Dr. Ronghua Ni (China)[1] (1. Fudan University)

2:20pm **34-3: A 0.18-µs-Locking-Time Fractional-N PLL with Stochastic Gradient Descent Tuning Curve Fitting, Initial Phase Error Zeroing, and Random DSM Achieving 44.4-fs Jitter at Near-Integer Channel**
» Mr. Hongzhuo Liu (China)[1], Prof. Wei Deng (China)[1], Prof. Haikun Jia (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

2:45pm **34-4: A 6.65-to-7.75GHz Fractional-N Digital PLL with Analog Pre-Distortion DTC Implementing 2nd/3rd-Order Calibration and Achieving -65.7dBc Fractional Spur and 154fs Integrated Jitter**
» Mr. Daxu Zhang (Japan)[1], Dr. Dingxin Xu (Japan)[1], Dr. Hongye Huang (Japan)[1], Mr. Waleed Madany (Japan)[1], Mr. Zezheng Liu (Japan)[1], Mr. Wenqian Wang (Japan)[1], Mr. Yuang Xiong (Japan)[1], Mr. Ashbir Aviat Fadila (Japan)[1], Mr. Duo Li (Japan)[1], Prof. Yuncheng Zhang (Japan)[1], Prof. Atsushi Shirane (Japan)[1], Prof. Kenichi Okada (Japan)[1] (1. Institute of Science Tokyo)

1:30pm **Data Converters IV -**
Session 35: High-Resolution and Noise-Shaping ADCs
Michelangelo
Chaired by: Prof. Lu Jie (China) and Prof. Shaolan Li (United States)

1:30pm **35-1: A 48x OSR 105.4-dB SNDR 24-kHz BW CT Zoom ADC with Reset Tri-level DWA and On-chip Negative-R Calibration**
» Mr. Yuyu Lin (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. Rui P. Martins (Macao)[1], Prof. Chi-Hang Chan (Macao)[1] (1. University of Macau)

Continued from **Wednesday, 16 April**

1:55pm

35-2: A 1V 9-86 fJ/conv.step 72.5dB-SNDR Level-Crossing Pipelined ADC with Triggered Sampling and Level Feedback

» Mr. Zexin Wang (China)[1], Mr. Lingxin Meng (China)[1], Prof. Menglian Zhao (China)[1], Ms. Mengyu Li (China)[1], Prof. Shuang Song (China)[1], Prof. zhichao tan (China)[1] (1. Zhejiang University)

2:20pm

35-3: A 95.9-dB SNDR 10-kHz BW 3rd-order VCO-based CT ΔΣ Modulator Using a Phase-Time Two-Step Quantizer

» Mr. Ken Li (United States)[1], Mr. Wei-En Lee (United States)[1], Mr. Xitie Zhang (United States)[1], Mr. Tian Xie (United States)[1], Mr. Tzu-Han Wang (United States)[1], Prof. Visvesh Sathe (United States)[1], Prof. Shaolan Li (United States)[1] (1. Georgia Institute of Technology)

2:45pm

35-4: A 20MHz-BW 12.3-ENOB NS SAR ADC with a 3rd-order Multi-Input Filter and a PVT-Robust Ratio-Based FIA

» Mr. Gabriele Zanoletti (Italy)[1], Mr. Gabriele Bè (Italy)[1], Mr. Michele Rocco (Italy)[1], Mr. Luca Ricci (Italy)[1], Ms. Alessia Ceroni (Italy)[1], Prof. Salvatore Levantino (Italy)[1], Prof. Andrea Leonardo Lacaita (Italy)[1], Prof. Luca Bertulessi (Italy)[1], Prof. Andrea Bonfanti (Italy)[1], Prof. Carlo Samori (Italy)[1] (1. Politecnico di Milano)

1:30pm

Biomedical Technologies and Applications II -

Session 36: Communication Computing and Sensing Techniques in Biomedical Systems

Aquitania

Chaired by: Soner Sonmezoglu (United States) and Prof. Kaiyuan Yang (United States)

1:30pm

36-1: RPG-HBC: Reconfigurable Passive Galvanic Human Body Communication for Bioelectronic Implants under Varying Channel Conditions

» Mr. Yonghee Chang (United States)[1], Mr. Wei Wang (United States)[1], Mr. Yiwei Zou (United States)[1], Prof. Kaiyuan Yang (United States)[1] (1. Rice University)

1:55pm

36-2: A Wearable Backscatter System Featuring Concurrent RF Harvesting and Bidirectional Communication with Commodity BLE Transceivers

» Mr. Ji Xiong (China)[1], Mr. Yongling Zhang (China)[1], Mr. Junzai Chen (China)[1], Mr. Xiaoyu Li (China)[1], Mr. Jinrui Zuo (China)[2], Prof. Yan Wang (China)[2], Prof. Xiaoyi Wang (China)[1], Prof. Jiangfeng Wu (China)[1], Prof. Miao Meng (China)[1] (1. Tongji University, 2. Fudan University)

2:20pm

36-3: A Wireless Biopotential Sensing Node with Simultaneous Body-Channel Communication by TX-Coupled 21 VPP Common-Mode Interference Suppression

» Mr. Yingjie Zhu (China)[1], Mr. Ruizhi Liu (China)[1], Mr. Yiqing Lan (China)[1], Dr. Yilong Dong (China)[1], Mr. Zhenyu Guo (China)[1], Ms. Ruohan Wu (China)[1], Ms. Yuxin Chen (China)[1], Prof. Longyang Lin (China)[1], Prof. Jerald Yoo (Korea, Republic of)[2], Prof. Jiamin Li (China)[1] (1. Southern University of Science and Technology, 2. Integrated Microsystems Laboratory Department of Electrical and Computer Engineering Seoul National University)

2:45pm

36-4: A Reconfigurable 0.69-1.02nJ/Classification Biomedical Al Processor for Intelligent Health Monitoring Devices

» Mr. Yuanzhe Zhao (Macao)[1], Mr. Yuheng Wang (Macao)[1], Mr. Zijian Wang (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. Rui P. Martins (China)[1], Prof. Chi-Hang Chan (Macao)[1], Prof. Minglei Zhang (Macao)[1] (1. University of Macau)

1:30pm

Digital Circuits and SoCs V -

Session 37: Machine Learning and Energy Efficient SoCs

Brittannic

Chaired by: Gregory Chen (United States) and Prof. Visvesh Sathe (United States)

1:30pm

37-1: (INVITED) Key, Value, Compress: A Systematic Exploration of KV Cache Compression Techniques

» Ms. Neusha Javidnia (United States)[1], Ms. Bita Darvish Rouhani (United States)[2], Prof. Farinaz Koushanfar (United States)[1] (1. University of California San Diego, 2. NVIDIA)

Continued from **Wednesday, 16 April**

2:20pm

37-2: A Phase-Locked Minimum-Energy-Point-Tracking Enabled by Unified-Clock-Power-and-Body-Bias Slack Regulation and PI-Ratio Based In-Situ Loop Gain Optimization with 97.4% Supply Voltage Margin Recovery at Minimum-Energy-Point in 28nm FDSOI

» Mr. Minhyeok Jeong (Korea, Republic of)[1], Mr. Hyungmin Gi (Korea, Republic of)[2], Mr. Minsik Cho (Korea, Republic of)[1], Mr. Mingyu Kim (Korea, Republic of)[1], Mr. Donggyu Kim (Korea, Republic of)[1], Mr. Sungyong Park (Korea, Republic of)[2], Mr. Woonjae Lee (Korea, Republic of)[2], Mr. Seonho Kim (Korea, Republic of)[2], Mr. Yeohoon Yoon (Korea, Republic of)[3], Mr. Shin Han (Korea, Republic of)[1], Mr. Donguk Seo (Korea, Republic of)[1], Prof. Jongmin Lee (Korea, Republic of)[4], Prof. Yoonmyung Lee (Korea, Republic of)[1] (1. Dept. of Electrical and Computer Engineering, Sungkyunkwan University, 2. Samsung Electronics, 3. Hyundai Motors Company, 4. Ajou University)

2:45pm

37-3: A High Accuracy and Ultra-Low Energy Environmental Sound Recognition Processor with Progressive Spectrogram Processing and Adaptive Weight Clustering based Online Learning

» Dr. Lujie Peng (China)[1], Mr. Xiben Jiao (China)[1], Mr. Zhiyi Chen (China)[1], Mr. Junyu Yang (China)[1], Mr. Rui Hong (China)[1], Mr. Longke Yan (China)[1], Mr. Yu Long (China)[1], Mr. Xiao Chen (China)[2], Mr. Xiaoyu Miao (China)[2], Prof. Zheng Wang (China)[1], Prof. Zhengning Wang (China)[1], Prof. Liang Zhou (China)[1], Prof. Liang Chang (China)[1], Prof. Shanshan Liu (China)[1], Prof. Tae Hyoung Kim (Singapore)[3], Prof. Jun Zhou (China)[1] (1. University of Electronic Science and Technology of China, 2. China Micro Semicon, 3. Nanyang Technological University)

3:10pm

Break

Grand Ballroom Foyer

3:35pm

Systems and Security III cont'd -

Session 33: Advancing System Designs with Chiplet Technology (CICC/CHISIC)

Grand Ballroom

Chaired by: Richard Dorrance (United States) and Mingu Kang (United States)

3:35pm

33-3 (BEST REGULAR PAPER CANDIDATE): A 68 TOPS/W, 256MB SRAM Sparse GEMM Accelerator Tiled Across 16, 4nm Near Memory Compute (NMC) Chiplets Disaggregated 2.5D System

» Dr. Srivatsa rangachar Srinivasa (United States)[1], Dr. Prerna Budhkar (United States)[1], Dr. Gauthaman Murali (United States)[1], Dr. Vui Cheng Chua (United States)[2], Mr. Paolo Aseron (United States)[2], Dr. Vinayak Honkote (United States)[1], Dr. Ravishankar Iyer (United States)[2], Mr. Nilesh Jain (United States)[2], Mr. Dileep Kurian (United States)[1], Ms. Anuradha Srinivasan (United States)[1], Dr. Tanay Karnik (United States)[1] (1. Intel Corp, 2. Intel)

4pm

33-4: (INVITED) 3D-IC Chiplet Integrated Power Supply with LDO, SCVR, and Buck DC-DC Converter

» Prof. Xiaosen Liu (China)[1], Mr. Xichen Sun (China)[1], Mr. Haozhe Zhang (China)[1], Prof. Yan Wang (China)[2] (1. Tsinghua University, 2. School of Integrated Circuits， Tsinghua University)

4:50pm

33-5: On-Chip Circuit Harness Enabling Probe-Less, Position-Invariant and Massive Testing of Chiplets via Die Front/Back-Side Capacitive Coupling

» Mr. Neelkamal Semwal (Singapore)[1], Dr. Luigi Fassio (Singapore)[1], Prof. Massimo Alioto (Singapore)[1] (1. Department of Electrical and Computer Engineering, National University of Singapore)

3:35pm

Wireless Transceivers and RF/mm-Wave Circuits and Systems VI cont'd -

Session 34: Design Techniques for RF/mmWave CMOS Phased-Locked Loops

Olympia

Chaired by: Hsieh-Hung Hsieh (Taiwan) and Aravind Nagulu (United States)

3:35pm

34-5: A 24.6-to-30.6GHz Magnetic-Isolated Sub-Sampling PLL with a Fast-Locking FLL Achieving 64.9fs Jitter, -253.3dB FoMJ, and -69.1dBc Reference Spur in 65nm CMOS

» Mr. Hanzhang Cao (China)[1], Ms. Chuqiao Wang (China)[1], Mr. Yanwei Liu (China)[1], Prof. Wen Wu (China)[2], Prof. Tongde Huang (China)[2], Prof. Xiaolong Liu (China)[1] (1. Southern University of Science and Technology, 2. Nanjing University of Science and Technology)

Continued from **Wednesday, 16 April**

4pm **34-6: A 22.4-25.6GHz Ping-Pong Sub-Sampling PLL Featuring Unified Supply Voltage and Balanced 2nd Harmonic Extraction Achieving 45.8fsrms Jitter and −254.3dB FoM**

» Dr. Yunbo Huang (China)[1], Prof. Zunsong Yang (China)[2], Dr. Hongyu Ren (China)[2], Prof. Rui P. Martins (China)[1], Prof. Yan Lu (China)[3], Prof. Nan Sun (China)[3], Prof. Nan Qi (China)[4], Prof. Yong Chen (China)[3] (1. University of Macau, 2. Institute of Microelectronics of the Chinese Academy of Sciences, 3. Tsinghua University, 4. Institute of Semiconductors, Chinese Academy of Sciences)

4:25pm **34-7: A 0.7-V 26.2-28.5 GHz Dual-Loop Double-Sampling PLL with Floating Capacitor OTA Based Gm-CP Achieving a 45.4-fsRMS Jitter**

» Dr. Jun Chang (China)[1], Dr. Hongzhi Liang (China)[1], Dr. Yixiao Luo (China)[1], Dr. Zeyu Peng (China)[1], Dr. Zhe Li (China)[1], Prof. Yi Shen (China)[1], Prof. Shubin Liu (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

3:35pm **Data Converters IV cont'd -**
Session 35: High-Resolution and Noise-Shaping ADCs
Michelangelo
Chaired by: Prof. Shaolan Li (United States) and Prof. Lu Jie (China)

3:35pm **35-5: A 110µW 99.5dB-SNDR 20kHz-BW Intrinsically Linear CTDSM with Hybrid Gm-Boosting OTA and Tri-Level FIR DACs**

» Ms. Xinhang Xu (China)[1], Mr. Yaohui Luan (China)[1], Mr. Jie Li (China)[1], Mr. Jihang Gao (China)[1], Mr. Kwok-Cheong Li (China)[1], Mr. Jiajia Cui (China)[1], Prof. Ru Huang (China)[1], Prof. Linxiao Shen (China)[1] (1. Peking University)

4pm **35-6: An 18-bit 183.9dB-FoMS,DR MES/Calibration-Free Scalable Zoom ADC using Fully Passive Coarse Modulator and Gain-Linearity-Enhanced FIA with Sub-1ppm-THD at Full Scale Input in 65-nm CMOS**

» Dr. Yuke Shen (China)[1], Prof. Shubin Liu (China)[1], Mr. Deao Wu (China)[1], Dr. Kui Wen (China)[1], Dr. Yanbo Zhang (China)[1], Prof. Yi Shen (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

4:25pm **35-7: A 90.1dB SNDR, 180.2dB FoMSNDR, 10kHz BW Gm-C-based ΔΣ ADC with Capacitive Input Feedforward and Duty-Cycled Gm Technique**

» Dr. Linran Zhao (United States)[1], Mr. Yiming Han (United States)[1], Dr. Yaoyao Jia (United States)[1] (1. The University of Texas at Austin)

4:50pm **35-8: A 0.0022\,mm^2, 2\,GS/s Resettable VCO-Based ADC Without Quantization Noise Shaping**

» Mr. Tao Lu (China)[1], Mr. Zixiang Liu (China)[1], Mr. Hao Yang (China)[1], Prof. Sai-Weng Sin (Macao)[2], Prof. Robert Bogdan Staszewski (Ireland)[3], Prof. Fujiang Lin (China)[1], Prof. Liheng Lou (China)[1], Prof. Yizhe Hu (China)[1] (1. University of Science and Technology of China, 2. University of Macau, 3. University college dublin)

3:35pm **Biomedical Technologies and Applications II cont'd -**
Session 36: Communication Computing and Sensing Techniques in Biomedical Systems
Aquitania
Chaired by: Soner Sonmezoglu (United States) and Prof. Kaiyuan Yang (United States)

3:35pm **36-5: An Energy-Efficient Healthcare Chest Patch Interface with Multi-Domain On-Sensor Computing and Inter-Sensor Windowing**

» Mr. Sanghyeon Cho (Korea, Republic of)[1], Mr. Jeonghoon Cho (Korea, Republic of)[1], Mr. Hyunjoong Kim (Korea, Republic of)[1], Mr. You Jang Pyeon (Korea, Republic of)[1], Mr. Dong Kwan Kang (Korea, Republic of)[1], Mr. Yonggi Kim (Korea, Republic of)[1], Mr. Eui Sung Jung (Korea, Republic of)[1], Prof. Hoon Eui Jeong (Korea, Republic of)[1], Prof. Jae Joon Kim (Korea, Republic of)[1] (1. Ulsan National Institute of Science and Technology)

4pm **36-6 (BEST STUDENT PAPER CANDIDATE): A Fully-Integrated Wireless Ingestible Drug Delivery Chip with Electrochemical Energy Harvesting and pH-Based MPPT**

» Mrs. So-Yoon Yang (United States)[1], Mr. Deniz Umut Yildirim (United States)[1], Dr. Saransh Sharma (United States)[1], Prof. Donghyeon Han (Korea, Republic of)[2], Dr. Rishabh Mittal (United States)[3], Mrs. Husna Ellis (United States)[1], Mr. Jaehong Jung (United States)[1], Mr. Eunseok Lee (United States)[1], Mr. Yubin Cai (United States)[1], Prof. Giovanni Traverso (United States)[1], Prof. Anantha P. Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. Chung-ang University, 3. MediaTek)

Continued from **Wednesday, 16 April**

4:25pm

36-7: A 0.7pArms Electrochemical Readout IC for Continuous Monitoring of Antibody Biologics in Upstream Biomanufacturing

» Mr. Hung-Yu Hou (United States)[1], Ms. Ya-Chen Tsai (United States)[1], Mr. Wei Foo (United States)[1], Ms. Yan-Ting Hsiao (United States)[1], Prof. Jun-Chau Chien (United States)[1] (1. University of California, Berkeley)

3:35pm

Digital Circuits and SoCs V cont'd -
Session 37: Machine Learning and Energy Efficient SoCs
Brittannic
Chaired by: Gregory Chen (United States) and Prof. Visvesh Sathe (United States)

3:35pm

37-4: CCE: A 28nm Content Creation Engine with Asymmetric Computing, Semantic-Driven Instruction Generation and Collision-free Outlier Mapper for Video Generation

» Dr. Chen Tang (China)[1], Ms. Zongle Huang (China)[1], Mr. Wenxun Wang (China)[1], Mr. Yifan He (China)[1], Mr. Shupei Fan (China)[1], Dr. Xiaoyu Feng (China)[1], Dr. Wenyu Sun (China)[1], Prof. Yongpan Liu (China)[1] (1. Tsinghua University)

4pm

37-5: A 22nm Resource-Frugal Hyper-Heterogeneous Multi-Modal System-on-Chip Towards In-Orbit Computing

» Dr. quan cheng (Japan)[1], Mr. qiufeng li (China)[2], Mr. Weirong Dong (China)[2], Mr. mingtao zhang (Japan)[1], Prof. Ruilin Zhang (Japan)[1], Prof. mingqiang huang (China)[2], Prof. Hao Yu (China)[2], Prof. yiyu shi (United States)[3], Prof. hiromitsu awano (Japan)[1], Prof. takashi sato (Japan)[1], Prof. Longyang Lin (China)[2], Prof. masanori hashimoto (Japan)[1] (1. Kyoto University, 2. Southern University of Science and Technology, 3. University of Notre Dame)

4:25pm

37-6: A 748 GOPS/W RISC-V SoC with Reconfigurable Custom Instructions via a Synthesized eFPGA with 1.8µs Configuration Time in 22nm FinFET

» Dr. Prashanth Mohan (United States)[1], Mr. Siddharth Das (United States)[1], Dr. Ken Mai (United States)[1] (1. Carnegie Mellon University)

4:50pm

37-7: E-NPU: A 34~126nJ/Class Event-Driven Adaptive Neural SoC with Signal-Dynamics-Aware Feature Clustering and Multi-model In-Memory Inference/Training for Personalized Medical Wearables

» Mr. Fengshi Tian (Hong Kong)[1], Mr. Jinbo Chen (China)[2], Mr. Kunming Shao (Hong Kong)[1], Ms. Zilu Liu (Hong Kong)[1], Mr. Jiakun Zheng (Hong Kong)[1], Mr. Hui Wu (China)[2], Mr. Chaoming Fang (China)[2], Ms. Xiaomeng Wang (Hong Kong)[1], Mr. Ziyang Shen (China)[2], Mr. Pingcheng Dong (Hong Kong)[1], Dr. Yuan Yao (Hong Kong)[1], Dr. Xuliang Wang (China)[3], Dr. Jie Yang (China)[2], Prof. Mohamad Sawan (China)[2], Prof. Chi-Ying Tsui (Hong Kong)[1], Prof. Kwang-Ting Cheng (Hong Kong)[1] (1. Hong Kong University of Science and Technology, 2. Westlake University, 3. Tsinghua University)

5:15pm

37-8: Opal: A 16nm Coarse-Grained Reconfigurable Array for Full Sparse ML Applications

» Mr. Po-Han Chen (United States)[1], Mr. Bo Wun Cheng (United States)[1], Mr. Michael Oduoza (United States)[1], Mr. Zhouhua Xie (United States)[1], Mr. Kalhan Koul (United States)[1], Mr. Sai Gautham Ravipati (United States)[1], Mr. Yuchen Mei (United States)[1], Mr. Rupert Lu (United States)[1], Mr. Alex Carsello (United States)[1], Prof. Mark Horowitz (United States)[1], Prof. Priyanka Raina (United States)[1] (1. Stanford University)

5:30pm

CHISIC WORKSHOP REGISTRANTS ONLY -
CHISIC Keynote 1: Chip to Chip Communication for Next Generation AI Datacenters
Olympia

6:15pm

CHISIC WORKSHOP REGISTRANTS ONLY -
CHISIC Networking Reception
Skyline Ballroom

Thursday, 17 April

7am **CHISIC WORKSHOP REGISTRANTS ONLY - Breakfast (provided)**
Skyline Ballroom

8am **CHISIC WORKSHOP REGISTRANTS ONLY - CHISIC Workshop**
Brittannic

10:05am **Break**
Grand Ballroom Foyer

10:20am **CHISIC WORKSHOP REGISTRANTS ONLY. - CHISIC Workshop**
Brittannic

12:20pm **Group Pictures**
Skyline Ballroom

12:25pm **.CHISIC WORKSHOP REGISTRANTS ONLY - Lunch Break (provided)**
Skyline Ballroom

1:25pm **CHISIC WORKSHOP REGISTRANTS ONLY - CHISIC Workshop**
Brittannic

3:25pm **Break**
Grand Ballroom Foyer

3:40pm **CHISIC WORKSHOP REGISTRANTS ONLY - CHISIC Workshop**
Brittannic

5pm **CHISIC WORKSHOP REGISTRANTS ONLY - CHISIC Workshop - Closing Ceremony**
Brittannic