2025 Program-at-a-Glance

Boston, Massachusetts, USA

Sunday, 13 April 2025

All Sunday sessions are included with conference registration

Olympia	*Michelangelo*	*Aquitania*	*Brittannic*	*Grand Ballroom*
9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 1:** Mastering LLMs: A Deep Dive into Software Models, Hardware Challenges, Security and Reliability	9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 2:** High Precision Converters and Digital Calibration Techniques	9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 3:** Security or Privacy From Hardware to Systems	**Educational Session 4:** Advanced Biomedical Interfaces 9:00 am-4:45 pm *(12:15 pm-3:15 pm break)*	**Circuits Insights** **For Senior undergraduate & Starting Graduate Students – Pre-registration required* 9:15 am-4:45 pm
5:00 pm-6:30 pm **SSCS Bingo Networking Night** *Skyline Ballroom*				

Monday, 14 April 2025

8:30 am-8:50 am **Welcome and Opening Remarks** *Grand Ballroom*
8:50 am-9:40 am **Session 1:** Keynote Session *Grand Ballroom*
9:40 am-10:05 am BREAK *Grand Ballroom Foyer*

Grand Ballroom	*Olympia*	*Michelangelo*	*Aquitania*	*Brittannic*
10:05 am-12:10 pm **Session 2:** Analog Building Blocks and Sensing Circuits	10:05 am-11:45 am **Session 3:** Voltage Controlled Oscillators and Power Amplifiers	10:05 am-11:45 am **Session 4:** SC-based Power Conversion	10:05 am-12:10 pm **Session 5:** Incremental ADCs	10:05 am-12:05 pm **Session 6:** Forum: Hardware and Architectural Strategies for Building Cutting-edge AI Platforms
12:00 pm-1:30 pm LUNCH BREAK (on own)				
1:30 pm-3:00 pm **Session 7:** Panel: Do we really need a linear-gain amplifier anymore?	1:30 pm-3:10 pm **Session 8:** Advancements in Low-Power Wireless Technologies	1:30 pm-3:10 pm **Session 9:** Power Converter Techniques	1:30 pm-3:10 pm **Session 10:** Emerging Paradigms for AI, HPC, and Edge Computation	1:30 pm-3:10 pm **Session 11:** ASIC and Accelerators
3:10 pm-3:35 pm BREAK *Grand Ballroom Foyer*				
3:35 pm-5:15 pm **Session 12:** Advancements in Low-Power, High-Performance Analog Sensing and Interface Technologies	3:35 pm-5:40 pm **Session 13:** High-Speed Nyquist ADCs	3:35 pm-5:15 pm **Session 9 (cont'd):** Power Converter Techniques	3:35 pm-5:15 pm **Session 10 (cont'd):** Emerging Paradigms for AI, HPC, and Edge Computation	3:10 pm-5:40 pm **Session 11 (cont'd):** ASIC and Accelerators
5:30 pm-7:30 pm **Welcome Reception & Best Paper Candidate Poster Session** *Skyline Ballroom*				

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Tuesday, 15 April 2025				
Grand Ballroom	***Olympia***	***Michelangelo***	***Aquitania***	***Brittannic***
8:00 am-9:40 am **Session 14:** Innovations in High-Performance Analog and Mixed-Signal Circuit Design	8:00 am-9:30 am **Session 15:** Panel: mmWave/THz Design: A New Paradigm or a Repeat of History with Faster Transistors?	8:00 am-9:40 am **Session 16:** Application-Specific Power Management	8:00 am-9:40 am **Session 17:** Next-Generation Systems: From Datacenters to the Edge	8:00 am-9:40 am **Session 18:** Digital Compute-in-Memory
9:40 am-10:05 am BREAK *Grand Ballroom Foyer*				
10:05 am-12:05 pm **Session 19:** Forum: Potential of Open Source Design for Analog/Mixed Signal IC Education	10:05 am-11:35 am **Session 20:** Panel: Wireline and Lightwave Interconnects - The Shifting Boundary in the AI Era	10:05 am-11:45 am **Session 16 (cont'd):** Application-Specific Power Management		10:05 am-11:45 am **Session 18 (cont'd):** Digital Compute-in-Memory
12:00 pm-1:30 pm **Session 21:** Keynote Luncheon Session (Registration required) *Skyline Ballroom*				
1:30 pm-5:15 pm **Session 22:** High Performance Transceivers	1:30 pm-3:10 pm **Session 23:** Cryogenic and Silicon Photonic ICs	1:30 pm-3:10 pm **Session 24:** Hybrid DC-DC Converters	1:30 pm-3:10 pm **Session 25:** High-speed Wireline and Optical Communication	1:30 pm-3:10 pm **Session 26:** Advanced Biopotential Interfaces
3:10 pm-3:35 pm BREAK *Grand Ballroom Foyer*				
3:35 pm-5:15 pm **Session 22 (cont'd):** High Performance Transceivers	3:35 pm-5:35 pm **Session 27:** Probabilistic Computing	3:35 pm-5:15 pm **Session 24 (cont'd):** Hybrid DC-DC Converters	3:35 pm-5:15 pm **Session 25 (cont'd):** High-speed Wireline and Optical Communication	3:35 pm-5:15 pm **Session 26 (cont'd):** Advanced Biopotential Interfaces
5:30 pm-6:30 pm **IEEE SSCS Young Professionals and Women in Circuits Mentoring Event** *Michelangelo*				
6:00 pm-8:00 pm **CICC Conference Reception & Industry Information Session** *Skyline Ballroom*				

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Wednesday, 16 April 2025				
8:30 am-9:40 am Keynote Session *Grand Ballroom*				
9:40 am-10:05 am BREAK *Grand Ballroom Foyer*				
Grand Ballroom	***Olympia***	***Michelangelo***	***Aquitania***	***Brittannic***
10:05 am-12:10 pm **Session 28:** Next-Generation Systems: Hardware for Quantum and Secure Computing	10:05 am-12:05 pm **Session 29:** Forum: Emerging Techniques for Phase Locked Loops	10:05 am-12:10 pm **Session 30:** Continuous-Time ADCs	10:05 am-11:45 am **Session 31:** Energy Efficient Wireline Interconnects	10:05 am-12:05 pm **Session 32:** Panel: The Impact of AI: A Job Creator or Destroyer?
12:00 pm- 1:30 pm LUNCH BREAK (on own)				
1:30 pm-3:10 pm **Session 33:** Advancing System Designs with Chiplet Technology (CICC/CHISIC)	1:30 pm-3:10 pm **Session 34:** Design Techniques for RF/mmWave CMOS Phased-Locked Loops	1:30 pm-3:10 pm **Session 35:** High-Resolution and Noise-Shaping ADCs	1:30 pm-3:10 pm **Session 36:** Communication Computing and Sensing Techniques in Biomedical Systems	1:30 pm-3:10 pm **Session 37:** Machine Learning and Energy Efficient SoCs
3:10 pm-3:35 pm BREAK *Grand Ballroom Foyer*				
3:35 pm-5:15 pm **Session 33 (cont'd):** Advancing System Designs with Chiplet Technology (CICC/CHISIC)	3:35 pm-4:50 pm **Session 34 (cont'd):** Design Techniques for RF/mmWave CMOS Phased-Locked Loops	3:35 pm-5:15 pm **Session 35 (cont'd):** High-Resolution and Noise-Shaping ADCs	3:35 pm-4:50 pm **Session 36 (cont'd):** Communication Computing and Sensing Techniques in Biomedical Systems	3:35 pm-5:40 pm **Session 37 (cont'd):** Machine Learning and Energy Efficient SoCs
5:30 pm-6:16 pm **CHISIC Keynote 1:** Chip to Chip Communication for Next Generation AI Datacenters **CHISIC WORKSHOP REGISTRANTS ONLY* *Olympia*				
6:15 pm-8:15 pm **CHISIC Networking Reception** **CHISIC WORKSHOP REGISTRANTS ONLY* ***Skyline Ballroom***				

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The below sessions are open to CHISIC Workshop registrants only.

To attend these sessions, please add the CHISIC Workshop item to your registration.

Thursday, 17 April 2025
7:00 am-8:00 am **Breakfast (provided)** *Skyline Ballroom*
8:00 am-10:05 am **CHISIC Workshop** *Brittannic*
10:05 am-10:20 am **Break** *Grand Ballroom Foyer*
10:20 am-12:20 pm **CHISIC Workshop** *Brittannic*
12:20 pm-12:25 pm **Group Pictures** *Skyline Ballroom*
12:25 pm-1:25 pm **Lunch Break (provided)** *Skyline Ballroom*
1:25 pm-3:25 pm **CHISIC Workshop** *Brittannic*
Break **3:25 pm-3:40 pm** *Grand Ballroom Foyer*
3:40 pm-5:00 pm **CHISIC Workshop** *Brittannic*
5:00 pm-5:05 pm **CHISIC Workshop - Closing Ceremony** *Brittannic*