
CICC
IEEE Custom Integrated Circuits Conference
22-25 March 2020 | Boston, MA

Sunday, March 22 ***All Sunday sessions are included with conference registration****					
9:00 am-4:45 pm	**Educational Session 1:** RF/mmW Power Amplifiers	**Educational Session 2:** Phase-Locked Loops	**Educational Session 3:** Transceivers (5G /IoT)	**Educational Session 4:** Data Converters and Interface Circuits	**MathWorks Sessions** (9:00 am-10:30 am)
Monday, March 23					
8:30 am-8:50 am	**Welcome and Opening Remarks**				
8:50 am-9:40 am	**Session 1:** Keynote Session				
9:40 am-10:00 am	**Break**				
10:00 am-12:00 pm	**Session 2:** Trust: Innovations in Security Circuits	**Session 3:** PLL and VCO Techniques	**Session 4:** Forum: Electronics for Vehicles of the Future	**Session 5:** System Oriented Design Foundations	
12:00 pm- 2:00 pm	**Keynote Luncheon**				
2:00 pm-3:45 pm (Break 3:45 pm-4:00 pm)	**Session 6:** Emerging Devices and Sensing Applications	**Session 7:** RF & mm-WAVE Circuits and Transceivers	**Session 8:** Analog Circuits and Systems	**Session 9:** Forum: IP Blocks: Challenges for Next Decade Complex SoCs	
4:00 pm-5:15 pm					
Tuesday, March 24					
9:00 am-11:35 am	**Session 12:** Data Converter Techniques	**Session 13:** Efficient Neural Network Acceleration	**Session 14:** DC-DC Converters		
11:35 am-1:30 pm	**Lunch Break**				
1:30 pm-3:15 pm (Break 3:15 pm-3:30 pm)	**Session 16:** Energy-Efficient Systems for Wearable, Implantable, and IoT Applications	**Session 17**: SoC Design: From Bits to Gigabits	**Session 18**: Ultra-low Power Wireless Transceivers	**Session 19**: Forum: Journey of a Startup	
3:30 pm-5:40 pm			**Session 20:** High-Speed Wireline Transceivers	**Session 21:** Forum: Advances in 5G and Wireless Systems	
Wednesday, March 25					
9:30 am-12:05 pm	**Session 23:** Oversampled Data Converters	**Session 24:** GaN and High-Voltage Power Converters	**Session 25:** Analog in Advanced Technologies	**Session 26:** Technology Oriented Design Foundations	
12:05 pm-2:00 pm	**Lunch Break**				
2:00 pm-2:15 pm	**Closing and Awards Ceremony**				

2020 IEEE Custom Integrated Conference is going virtual!

The IEEE Custom Integrated Circuits Conference is a premier conference devoted to IC development. The conference program is a blend of oral presentations, exhibits and forums. The conference sessions present original first published technical work and innovative circuit techniques that tackle practical problems. CICC is the conference to find out how to solve design problems, improve circuit design techniques, get exposure to new technology areas, and network with peers, authors and industry experts.

There are 3 days of Technical Sessions that include lecture presentations addressing state of the art developments in integrated circuit design. The Educational Sessions are a full day of tutorials instructed by recognized invited speakers. The Forums are presented throughout the conference to enrich the learning experience of the attendees. The Forums are presented by leaders from the IC industry. CICC includes an Exhibits Hall that is open in the evenings where Semiconductor manufacturers, software tool suppliers, silicon IP providers, design-service houses, and technical book publishers offer displays and demonstrations of their products. CICC is sponsored by the IEEE Solid-State Circuits Society and technically co-sponsored by the IEEE Electron Devices Society.

Visit our website at www.ieee-cicc.org

IEEE CICC is sponsored by:

IEEE

SSCS
IEEE Solid-State Circuits Society

Steering Committee

General Chair
Hua Wang, Georgia Institute of Technology

Conference Chair
Fa Foster Dai, Auburn University

Technical Program Chairs
Christophe Antoine, Analog Devices
Samuel Palermo, Texas A&M

Solid State Circuits Society Representative
Hua Wang, Georgia Institute of Technology

Treasurer
Kimo Tam, Analog Devices

Past Chairman and Strategic Development Chair
Alessandro Piovaccari, Silicon Laboratories
Don Thelen, ON Semiconductors

Conference Coordination
John Teehan, CMP, IEEE MCE
Danielle Corrigan, IEEE MCE

Organizing Committee

Special Sessions
Shahriar Mirabbasi, University of British Columbia

Best Papers and Awards
Colin McAndrew, Freescale Semiconductor

Sponsorship and Exhibits
Stefano Pietri, NXP Semiconductors

Outreach
Mohammad Hekmat, Samsung

Mentorship
Julian Tham, Cypress Semiconductors

Technical Program Committees

Analog Circuits and Techniques
Chair, Sudhakar Pamarti, UCLA
Co-chair, Nagendra Krishnapura, IIT Madras
Ping Gui, Southern Methodist University (SMU)
Antonio Liscidini, University of Toronto
Mark Oude Alink, University of Twente
Hiroki Ishikuro, Keio University
Ivan O'Connell, University College Cork
Ion Tesu, Silicon Laboratories
Jiangfeng Wu Tongji, University Shanghai China
Stefano Pietri, NXP Semiconductors
Tolga Dinc, TI

Data Converters
Chair, Nima Maghari, University of Florida
Co-Chair, Mike Chen, University of Southern California
Nan Sun, The University of Texas at Austin
Jun Cao, Broadcom
Delong Cui, Broadcom
Yunzhi Dong, Analog Devices
Seung-Tak Ryu, KAIST
John Khoury, Silicon Laboratories
Ayman Shabra, MediaTek
Gil Engel, Analog Devices
Baradwaj Vigraham, Maxlinear
Lukas Kull, IBM
Filip Tavernier, KU Leuven
Hung-Chu Vanessa Chen, Carnegie Mellon University

Design Foundations
Chair, Paolo Miliozzi, Maxlinear
Co-Chair, Charles Augustine, Intel Circuit Research Lab
Colin McAndrew, Freescale Semiconductor
Jaydeep P Kulkarni, The University of Texas at Austin
Farhana Sheikh, Intel Circuit Research Lab
Mitsuhiko Igarashi, Renesas Electronics Corporation
Swaroop Ghosh, Penn State University
Shinya Kajiyama, Hitachi Xuan

(Silvia) Zhang, Washington University in St. Louis
Luca Daniel, Massachusetts Institute of Technology

Digital Circuits, SoCs, and Systems
Chair, Arijit Raychowdhury, Georgia Institute of Technology
Co-Chair, Carlos Tokunaga, Intel Corporation
Elkim Roa, Universidad Industrial de Santander
Shreyas Sen, Purdue University
Zhengya Zhang, University of Michigan
Gregory Chen, Intel Corporation
Rajiv Joshi, IBM T. J. Watson Research Center
Saad Bin, Nasir Qualcomm
Brian Zimmer, Nvidia

Emerging Technologies, Systems and Applications
Chair, Jerald Yoo, National University of Singapore
Co-Chair, Kaushik Sengupta, Princeton
Firooz Aflatouni, University of Pennsylvania
Mahsa Shoaran, Cornell University
Steven Bowers, University of Virginia
Drew Hall, University of California San Diego
Marco Tartagni, University of Bologna
Abhishek Bandyopadhyay, Analog Devices
Kiichi Nitsu, Nagoya University
Ulkuhan Guler, Worcester Polytechnic Institute

Power Management
Chair, Hanh-Phuc, University of California San Diego
Co-Chair, Dina El-Damak USC
Mehdi Kiani, Penn State University
Yan Lu, University of Macau
Mike Mulligan, Silicon Laboratories
Patrick Mercier,University of California San Diego
Tufan Karalar, Istambul TU
John Pigott, NXP Semiconductors
Chunlei Shi, Qualcomm
Eric Soenen, TSMC
Jason Stauth, Dartmouth College
Saurav Bandyopadhyay, Texas Instruments

Wireless Transceivers and RF/mm-Wave Circuits and Systems
Chair, Yanjie Wang, South China University of Technology
Co-Chair, Woogeun Rhee, Tsinghua University
Debopriyo Chowdhury, Broadcom
Amr Fahim, Inphi Corporation
Wanghua Wu, Samsung
Jane Gu, University of California, Davis
John Long, University of Waterloo
Hossein Lavasani, Qualcomm
Yahya Tousi, University of Minnesota
Aritra Banerjee, IMEC
Payam Heydari, University of California Irvine
Jacques “Chris” Rudell, University of Washington
Swaminathan Sankaran, Texas Instruments

Wireline and Optical Communications Circuits and Systems

Chair, Tod Dickson, IBM T.J. Watson
Co-Chair, Mayank Raj, Xilinx
Xiang Gao, Credo Semiconductor
Tzu-Chien Hsueh, University of California, San Diego
Mozhgan Mansuri, Intel
Mohammad Hekmat, Samsung
Tejasvi Anand, Oregon State University
Shahriar Mirabbasi, University of British Columbia
Sudip Shekhar, University of British Columbia
K. R. Kumar Lakshmikumar, Cisco Systems

Sunday, March 22
Educational Sessions (Included in registration)

Sunday, March 22, 2020, 09:00 AM–12:15 PM

Educational Session 1: RF/mmW Power Amplifiers

Session Chair: Debo Chowdhury, Broadcom
Session Co-Chair: Carlos Tokunaga, Intel Corporation

09:00 AM

ES1-1
High Efficiency mm-Wave Power Amplifiers in CMOS-SOI and SiGe for 5G
Peter Asbeck, UCSD

5G NR waveforms pose significant challenges for power amplifiers, as a result of their high peak-to-average power ratios, high bandwidths and requirements for low EVM – without the use of digital predistortion. CMOS-SOI and SiGe HBT technologies can attain the output power levels needed for most 5G mm-wave applications (Psat to above 23dBm). This talk will review device considerations impacting power and efficiency of mm-wave PAs, and presents 5G amplifier designs using Doherty, outphasing and hybrid designs to increase efficiency to above 25% at 6dB backoff. Design techniques for integration of PA, LNA and switches for mm-wave front-ends are also discussed.

10:30 AM

Break

10:45 AM

ES1-2
High Power Generation for mm-Wave 5G Power Amplifiers in Deep Submicron Planar and FinFET Bulk CMOS
Saeid Daneshgar, Intel

The required output power of power amplifiers (PAs) in 5G mm-Wave wireless transmitters is estimated to vary in the range of 18 to 24dBm across handset, access point, base station, and backhaul applications. A common perception within the industry is that at such power levels, low-cost bulk CMOS is inadequate in efficiency and there is a need for specialized technologies such as SOI or GaN. This tutorial attempts to allay such concerns and presents the key techniques for high power, high efficiency mm-Wave 5G PA design in deep submicron planar and FinFET bulk CMOS processes. It covers the design steps of reliable high power generation all the way from transistor level layout to active and passive on-chip power combining followed by a prediction of saturated output power (Psat) and its corresponding maximized power added efficiency (PAE) for a 3-stage PA. Finally, the tutorial will conclude with the measured results of two 39GHz PA prototypes in 16nm FinFET and 28nm planar bulk CMOS processes.

12:15 PM

Lunch Break

01:30 PM

ES1-3
Digital Power Amplifiers and Transmitters Based on RF Digital-to-Analog Converter

Sangmin Yoo, Michigan State University

In the era of the internet of things (IoT) and 5G communication, small, linear, and power-efficient wireless power amplifiers (PAs) and transceivers are critical for the small form factor, high-data throughput, and extended battery life of many mobile devices. On the other hand, innovations in analog/RF circuits have been driven by rapidly-evolving semiconductor technology in line with Moore's law. Digital PA and transmitter (Tx), based on RF digital-to-analog converter (DAC) architecture, have shown great promises for Tx systems with small area and excellent energy efficiency. The digital PA and Tx architecture, mostly based on digital circuits and switches, directly benefits from the advances in state-of-the-art nanometer-scale CMOS technology. The future of digital PA/Tx in wireless systems is not far away. This talk will give an introduction to the digital PA, and also cover recent advances, directions, and benefits that the wireless digital PA/Tx will bring about. Recent design examples will also be discussed. A polar switched-capacitor (SC) digital PA with 30dBm peak POUT demonstrates several efficiency peaks down to 18dB power backoff (PBO) associated with efficiency boosting techniques such as class-G, Doherty, and time-interleaving. A complete quadrature SC digital Tx with 13dBm peak POUT demonstrates a very small area and a low power consumption. These recent digital PA and digital Tx prototypes also show a great linearity of <-40dB EVM over >20dB POUT range without any digital predistortion (DPD) for an 802.11 signal.

03:00 PM

Break

03:15 PM

ES1-4
Envelope Tracking for 5G and mm-wave Power Amplifiers

Johana Yan, Maxentric

The demand for high data rates and better throughput has driven 5G communication systems to use higher order modulations. To overcome the efficiency degradation in power amplifiers in the presence of such waveforms, advance power amplifier architectures are needed. Among them is the envelope tracking power amplifier (ETPAs). In this talk, ETPAs based on both analog and digital modulators will be described and compared. Analog modulators, with hybrid architectures of different switching and linear stages in parallel and series configurations, and digital modulators, producing envelope approximates use as power DACs, multi-switchers, or tap-changers, are compared in terms of their performance merits (waveform fidelity, bandwidth, efficiency, etc), with emphasis on 5G applications. ETPAs designs and considerations for enabling digital communication systems with multi-beam/multi-channel transmission will be discussed. Linearization techniques for both analog and digital ETPAs and multi-beam/multi-channel operation will be shown.

Sunday, March 22, 2020, 09:00 AM–12:15 PM

Educational Session 2: Phase-Locked Loops

Session Chair: Woogeun Rhee, Tsinghua University
Session Co-Chair: Sudip Shekhar, University of British Columbia

09:00 AM

ES2-1
Beyond All-Digital PLL for RF and Millimeter-Wave Frequency Synthesis

Robert Staszewski, University College Dublin, Ireland

The past several years has seen proliferation of all-digital phase-locked loops (ADPLL) for RF, mm-wave and high-performance frequency synthesis due to their clear benefits of flexibility, reconfigurability, transfer function precision, settling speed, frequency modulation capability, and amenability to integration with digital baseband and application processors. When implemented in nanoscale CMOS, the ADPLL also exhibits advantages of better performance, lower power consumption, lower area and cost over the traditional analog-intensive charge-pump PLL. In a typical ADPLL, a traditional VCO got directly replaced by a digitally controlled oscillator (DCO) for generating an output variable clock, a traditional phase/frequency detector and a charge pump got replaced by a time-to-digital converter (TDC) for detecting phase departures of the variable clock versus the frequency reference (FREF) clock, and an analog loop RC filter got replaced with a digital loop filter. The conversion gains of the DCO and TDC circuits are readily estimated and compensated using ‘free’ but powerful digital logic.

10:30 AM

Break

10:45 AM

ES2-2
Basics of Closed- and Open-Loop Fractional Frequency Synthesis

Sudhakar Pamarti, University of California, Los Angeles

Fractional frequency synthesis is employed in a wide variety of applications, and the circuits that realize fractional frequency synthesis come in several forms. This talk presents the basics of fractional frequency synthesis by roughly grouping them into closed loop approaches such as those based on phase locked loops, and open loop approaches such as those based on fractional dividers and digital-to-phase converters. The talk will describe how these systems work, focusing on commonalities such as the use of digital delta sigma modulators, and on unique differences. The talk will also explore metrics such as phase noise, jitter, and spurious tones in these systems using examples wherever appropriate.

12:15 PM

Lunch Break

01:30 PM

ES2-3
Low-Spur PLL Architectures and Techniques
Mike Shuo-Wei Chen, University of Southern California

One key design objective of a frequency synthesizer is to minimize the spurious tones, as they can degrade the overall jitter performance or cause other unwanted system-level impairments. In this tutorial, we will examine the sources of the spurious tone generation in different PLL architectures and operation modes. We will overview several design techniques to mitigate the spurious tones. Lastly, we will go over several real PLL design examples that demonstrate low-spur performances.

3:00 PM

Break

03:15 PM

ES2-4
Subsampling PLLs for Frequency Synthesis and Phase Modulation
Nereo Markulic, IMEC, Leuven, Belgium

The tutorial starts with a basic/introductive overview of modern frequency synthesis techniques, delivering basic operation theory in an intuitive fashion. A point of attention is in this context brought to recent subsampling PLL architecture. This architecture overcomes the performance boundaries typically encountered in classical implementations and is redefining today's state-of-the state of art in frequency synthesis. We will try to explain why. The following part of the tutorial explores the subsampling loop in context of state-of-the art fractional synthesis and phase modulation. We show how to enable fractional-N multiplication modes, while retaining benefits of low-noise subsampling operation. This can be achieved by introducing digital-to-time converter (DTC)-based time domain signal processing. We will discuss potential limitations of this block, and how to overcome them in the analog, or in the digital domain. The versatility of the DTC-based subsampling PLL will further be discussed in context of phase/frequency modulation, which is crucial for accurate polar signaling. We will investigate classical loop-bandwidth limitations and explore how two-point modulation principles can elegantly be applied in context of the explored loop. We will openly discuss potential weak-points of this environment – and how to address them. This talk insists on an intuitive, rather than a strict, mathematical approach to PLLs. It starts from the basic concepts and then gradually expands in complexity, while clearly highlighting the key ideas and pointing to state-of-the-art embodiments.

Sunday, March 22, 2020, 09:00 AM–12:15 PM

Educational Session 3: Transceivers (5G /IoT)

Session Chair: Yanjie Wang, South China University of Technology
Session Co-Chair: Arijit Raychowdhury, Georgia Institute of Technology
Session Co-Chair: Chris Rudell, University of Washington

09:00 AM

ES3-1
5G RF Transceiver Design for EN-DC and MmWave

Jongwoo Lee, Samsung

To carry on the explosion of mobile data traffic, cellular networks have evolved to enhance air capacity with emerging 5G New Radio (NR) technologies. By 2020 demand and need for the mobile broadband will be very high and existing system will not be able to fulfill the user demand globally. Thanks to carrier aggregation (CA), higher order modulation up to 1024 QAM, and advanced MIMO techniques, the NR devices can attain up to several Gb/s peak data rate. The demand for high bandwidth has created a need for exploring high-frequency spectrum over 3 GHz while sustaining legacy LTE bands for LTE-NR dual connectivity (EN-DC). To increase the total aggregated bandwidth, a sophisticated CA operation is mandatory. The important thing is that hundreds of the existing LTE-A CAs still need to be supported. In addition, supporting legacy 2G/3G/4G radio operation is also critical for commercial global roaming. Because the user equipment (UE) requires small form-factor and low power consumption, a single-chip RF transceiver is essential to cover both NR and legacy protocols, simultaneously. To accelerate the 5G main features such as enhanced mobile broadband (eMBB) and ultra-reliable low-latency communications (URLLC), 5G mmWave communication system will be capable to provide low latency , high speed internet connection to the users across the globe in an efficient manner.

10:30 AM

Break

10:45 AM

ES3-2
Design of RF Transceivers for Medical Applications in 5G/IoT Era

Zhihua Wang, Tsinghua University

In the upcoming 5G era, mobile communication system can provide extremely high speed, extremely low latency, and almost unlimited addresses for everything in the universe. On the other hand, with the aging of the population and the improvement of people's living standards, the requirements for health and medical care are becoming more and more urgent and effective. The demand of medical electronic devices, which is one of the important types of IoT in 5G era, to make the medical devices smaller and smarter, will be one of the driving force of integrated circuits and systems. The implantable medical devices (IMD's), which are fully or partially implanted in the human bodies through surgeries, have a series of strict technical requirements including the choice of frequency and bandwidth, low power consumption, data rate, signal modulation method, disturbing and interference etc. This lecture focuses on a recently proposed technique in the art of radio transceiver design to reduce power consumption and area occupation. A set of miniature IMD's have been implemented using this ultra-low power transceiver which can be integrated in different application specific systems-on-a-chip (SoC's).

12:15 PM

Lunch Break

01:30 PM

ES3-3
Body Area Network – Connecting Things Together Around the Human Body

Jerald Yoo, National University of Singapore

Body Area Network (BAN) provides an attractive means for continuous and pervasive health monitoring, yet its unique and harsh environment gives circuit designers many challenges. As human body absorbs the majority of RF energy around GHz band, existing RF radio may not be an ideal for communications between and on-body sensors. In order to solve the issues, this education session talk presents the Body

Coupled Communication (BCC)-based BAN. The BCC BAN utilizes human body itself as a communication medium, which has orders of magnitude less pathloss when compared to RF based BAN. We will cover three types of BCC-BAN: 1) capacitive coupling, 2) magnetic coupling and 3) galvanic coupling. For each type, we will explorer its channel characteristics followed by design considerations and transceiver implementation examples. I will then discuss what circuit designers should consider in such non-conventional environments. Low energy circuit techniques to overcome their limitations will also be discussed. We will then review their various system aspects of the BAN, including powering up the wearables using the wearable BAN.

03:00 PM

Break

03:15 PM

ES3-4
Fundamentals of Modern mmW Radars
Brian Ginsburg, Texas Instruments

mm-Wave radars are a key sensor for modern automotive driver assistance systems and have emerging uses in building and factory automation, as well as human interactive motion sensing. This tutorial will cover the basic radar parameters including resolution, accuracy, and maximum range, and show how those are linked to fundamental system specifications. Frequency modulated continuous wave (FMCW) is the dominant waveform. Detailed examples will be given of a fast chirp FMCW implementation. Finally, recent radar advances, including PMCW modulation, imaging radars, and integrated antennas will be discussed.

Sunday, March 22, 2020, 09:00 AM–12:15 PM

Educational Session 4: Data Converters and Interface Circuits

Session Chair: Nan Sun, The University of Texas at Austin
Session Co-Chair: Nima Maghari, University of Florida

09:00 AM

ES4-1
Backend Improvement in ΔΣ ADCs
Nima Maghari, University of Florida

Delta-Sigma modulators are widely used in applications ranging from low frequency and audio to wideband wireless receivers. Several key advantages such as anti-aliasing filtering, reduced sensitivity to some circuit non-idealities such as lowered opamp gain requirement, wide dynamic range among others have contributed to the success of these structures. However, as the move towards higher data rates and wide bandwidth is becoming more dominant, the limiting factor of delta-sigma ADCs becomes the achievable sampling speed to maintain the efficiency of the oversampling ratio. Consequently, comprehensive efforts have been dedicated in improving the backend quantization and excess loop delay compensation in the past decade leading to various innovations in circuit and system level. However, a comprehensive study of the behavior, the advantages and drawbacks of these techniques is missing from the literature and textbooks. In this talk, the effects of back-end quantizer in ΔΣ ADCs are discussed in details, the new emerging quantizers and excess loop-delay compensation schemes are presented and

the advantages and drawbacks of each will be analyzed.

10:30 AM

Break

10:45 AM

ES4-2
Ringamp: The Scalable Amplifier We've All Been Waiting For?
Ben Hershberg, IMEC

Conventional opamps have not scaled gracefully into nanoscale CMOS, and the quest for a general-purpose replacement continues to challenge the research community. This has fundamentally reshaped the field of ADCs in the last decade, where designers have been forced toward architectures that avoid linear amplifiers as much as possible. This evolutionary pressure has in many ways been a boon, stimulating new approaches and ways of thinking. But it also raises the question: what opportunities for creativity and innovation did we lose when we left opamps behind? What impact would a viable successor have on the ADC landscape? Ring amplification is an emerging technique that offers the possibility of high efficiency, high performance, scalable, and general-purpose switched capacitor amplification. This talk will begin with a discussion of what exactly a "ringamp" is, how it works, and why it works so well. We will then go through a practical design example and see how the modelling and validation process is fundamentally different from conventional opamp design. We will also consider challenges such as PVT robustness. With a foundation in place, we will expand to considerations of topology choices and performance enhancements that can be used to build the optimal ringamp for a given application.

12:15 PM

Lunch Break

01:30 PM

ES4-3
High Speed Digital-to-Analog Converters – A Tutorial
Gabriele Manganaro, Analog Devices

Current-steering Digital-to-Analog Converters (DACs) are commonly the architecture of choice for analog signal synthesis from MHz to sub-THz frequencies in a variety of applications ranging from wireless and wired communication, instrumentation, imaging to defense among others. This tutorial will guide the audience from the basic architectural concepts and simplest circuit implementations to the different types of impairments and ways to mitigate them. Trade-offs, circuits and layout techniques to overcome them, and examples of actual high-speed DACs embodying the different concepts will be discussed in a intuitive fashion, providing the audience with selected literature references for deepening the material as needed.

3:00 PM

Break

03:15 PM

ES4-4
Analog Front-ends for Large Scale Neural Recording
Ross Walker, University of Utah

In the last 60 years, microfabrication techniques developed for ICs have driven exponential growth in the

number of individual brain cells that can be recorded from simultaneously, albeit with a shallower slope compared to Moore's law (doubling every ~7 years). At the current state of the art, analog front-ends for neural recording have become a major bottleneck in understanding the brain, and are also seen as a limitation for potential human applications of large scale neural interfacing. This tutorial will first review established solutions for signal conditioning and data conversion in neural recording, including both architecture and circuit implementation. New techniques that march the data converter closer to the electrode sites will be presented and analyzed, including direct delta-sigma conversion and rapidly multiplexed Nyquist approaches. Tradeoffs in power, area, and system complexity will be highlighted, as well as application specific design criteria that motivate further innovation.

Sunday, March 22, 2020, 09:00 AM–10:30 AM

MathWorks Sessions (Included in registration)

09:00 AM

Introduction to IBIS-AMI

Mike Mayer
MathWorks

The speed of serial communication links (SerDes) continues to climb, and design complexity grows with it. IBIS-AMI models are a standardized way for SerDes designers to share a behavioral model of their chip with downstream system designers such as board-level signal integrity engineers. Creating IBIS-AMI models is now part of the workflow for SerDes designers, but it is a complex and time consuming task which requires knowledge of the IBIS-AMI specification, SerDes, signal integrity, and C programming. This talk covers the background of IBIS-AMI, the basics of the specification, and approaches to generating standard models more efficiently.

- What is IBIS and IBIS-AMI?
- Why behavioral models?
- IBIS History
- IBIS-AMI for SerDes
- IBIS-AMI for DDR5
- Creating IBIS-AMI models
- Using IBIS-AMI models

Monday, March 23

Monday, March 23, 2020, 08:30 AM–08:50 AM

Welcome and Opening Remarks

Monday, March 23, 2020, 08:50 AM–09:40 AM

Session 1: Keynote Session

08:50 AM

Vivek De, Intel Fellow, Director of Circuit Technology Research in Intel Labs, Intel

Title: Attack-Resistant Energy-Efficient SoC for Smart & Secure IoT

Abstract: We will discuss SoC design challenges and opportunities for smart and secure cyberphysical systems in the emerging world of IoT, focusing on two distinct areas: (1) how to deliver uncompromising performance and user experience while minimizing energy consumption, and (2) how to provide cryptographic-quality “roots of trust” in silicon and resistance to physical side channel attacks with minimal overhead. We will present SoC designs that span a wide range of performance and power across diverse platforms and workloads, and achieve robust near-threshold-voltage (NTV) operation in nanoscale CMOS. We will discuss techniques to overcome the challenges posed by device parameter variations, supply noises, temperature excursions, aging-induced degradations, workload and activity changes, and reliability considerations. True Random Number Generator (TRNG) and Physically Unclonable Function (PUF) circuits, the two critical silicon building blocks for generating dynamic and static entropy for encryption keys and digital fingerprints, respectively, will be presented. We will also discuss power and electromagnetic physical side-channel-attack detection and mitigation techniques for enabling robust hardware security.

Biography: Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 295 publications in refereed international conferences and journals with a citation H-index of 79, and 227 patents issued with 32 more patents filed (pending). He received an Intel Achievement Award for his contributions to an integrated voltage regulator technology. He is the recipient of the 2019 IEEE Circuits and System Society (CASS) Charles A. Desoer Technical Achievement Award for “pioneering contributions to leading-edge performance and energy-efficient microprocessors & many-core system-on-chip (SoC) designs”. He received the 2017 Distinguished Alumnus Award from the Indian Institute of Technology (IIT) Madras. He received a B.Tech from IIT Madras, India, a MS from Duke University, Durham, North Carolina, and a PhD from Rensselaer Polytechnic Institute, Troy, New York, all in Electrical Engineering. He is a Fellow of the IEEE.

09:40 AM

Break

Monday, March 23, 2020, 10:00 AM–11:45 AM

Session 2: Trust: Innovations in Security Circuits

Session Chair: Elkim Roa, Universidad Industrial de Santander
Session Co-Chair: Carlos Tokunaga, Intel Corporation

This session features papers in security circuits for trustworthy systems. The first two papers showcase authentication systems, one with a confined signal within the body, followed by a system using visible light-based interrogation. The last two papers feature two security entities, an AES-256 engine resilient to deep learning attacks, and a bit-error free SRAM-based physically unclonable function.

10:00 AM

Introduction: Trust: Innovations in Security Circuits

10:05 AM

2-1
A 415 nW Physically and Mathematically Secure Electro-Quasistatic HBC Node in 65nm CMOS for Authentication and Medical Applications

Shovan Maity[1]; Nirmoy Modak[1]; David Yang[1]; Shitij Avlani[1]; Mayukh Nath[1]; Josef Danial[1]; Debayan Das[1]; Parikha Mehrotra[1]; Shreyas Sen[1]
[1]School of Electrical and Computer Engineering, Purdue University

In this paper, we design a secure HBC SoC node, which uses EQS-HBC for physical security and an AES-256 engine for mathematical security. The SoC consumes 415nW power with an active power of 108nW for a data rate of 1kbps, suitable for applications such as secure authentication and remote physiological monitoring applications.

10:30 AM

2-2
An Authentication IC with Visible Light Based Interrogation in 65nm CMOS

Edward Lee[1]; Nael Mizanur Rahman[1]; Venkata Chaitanya Krishna Chekuri[1]; Saibal Mukhopadhyay[1]
[1]Georgia Institute of Technology

An authentication IC with Visible-Light based power and data transfer for interrogation consuming 2.29 µW of standby power is presented in 65nm CMOS. An on-chip regulator boosts optical energy harvested by external diodes to power encryption and sensing. On-chip light sensing using CMOS photodiodes achieves 53.8kbps data download rate. An 64-bit PRINCE cipher is implemented for authentication.

10:55 AM

2-3
Deep Learning Side-Channel Attack Resilient AES-256 using Current Domain Signature Attenuation in 65nm CMOS

Debayan Das[1]; Josef Danial[1]; Anupam Golder[2]; Santosh Ghosh[3]; Arijit Raychowdhury[2]; Shreyas Sen[1]

[1]Purdue University; [2]Georgia Institute of Technology; [3]Intel Labs

This paper presents a current domain signature attenuation(CDSA) circuit fabricated in 65nm CMOS to prevent deep-learning power side-channel analysis(DLSCA) attacks on cryptographic ICs.The countermeasure embeds the crypto core(AES256) within the CDSA hardware to suppress the critical signature by >350x,before it reaches the power supply pin.Measurements show that 256-class deep-neural-network(DNN) model can be fully trained(>99.9% test accuracy) using

11:20 AM

2-4
A 0.5-V 2.07-fJ/b 497-F2 EE/CMOS Hybrid SRAM Physically Unclonable Function with < 1E-7 Bit Error Rate Achieved through Hot Carrier Injection Burn-in

Kunyang Liu[1]; Hongliang Pu[1]; Hirofumi Shinohara[1]

[1]Waseda University

This paper describes an EE/CMOS hybrid SRAM PUF with key features including (1) zero bit error at all VT corners from 0.5 to 0.7 V and −40 °C to 120 °C via HCI burn-in; (2) a data latching scheme using the hybrid SRAM characteristic, which enables low-voltage operation down to 0.5 V; (3) high energy efficiency with 2.07 fJ/b core energy at 0.5 V; and (4) a small footprint of 497 F2.

Monday, March 23, 2020, 10:00 AM–11:45 AM

Session 3: PLL and VCO Techniques

Session Chair: Wanghua Wu, Samsung
Session Co-Chair: Amr Fahim, Broadcom

10:00 AM

Introduction: PLL and VCO Techniques

10:05 AM Best Student Paper Candidate

3-1
A 7.7~10.3GHz 5.2mW −247.3dB-FOM Fractional-N Reference Sampling PLL with 2nd Order CDAC Based Fractional Spur Cancellation In 45nm CMOS

Dongyi Liao[1]; Fa Foster Dai[1]

[1]Auburn University

In this paper, a fractional-N reference sampling PLL (RSPLL) with capacitor digital-to-analog converter

(CDAC) based quantization error canceller is presented. The prototype chip was fabricated in a 45nm PDSOI CMOS process. Measurement showed an output frequency range covering 7.7~10.3GHz with an integrated jitter of 190fs and an in-band fractional spur level of -56dBc. The entire PLL consumes 5.2mW and achieves a FoM of -247.3dB.

10:30 AM Best Student Paper Candidate

3-2:
A Wideband 180-GHz Phase-Locked-Loop Based MSK Receiver

Shenggang Dong[1]; Ibukunoluwa Momson[1]; Sandeep Kshattry[1]; Pavan Yelleswarapu[1]; Wooyeol Choi[1]; Wooyeol Choi[2]; Kenneth O[1]

[1]The University of Texas at Dallas; [2]Oklahoma State University

A 180 GHz mixer-first phase-locked-loop based MSK receiver is demonstrated in 65-nm CMOS with -24dBm input sensitivity at a BER

10:55 AM

3-3
A 0.55mW Fractional-N PLL with a DC-DC Powered Class-D VCO Achieving Better than -66dBc Fractional and Reference Spurs for NB-IoT

Hossein Rahmanian Kooshkaki[1]; Patrick Mercier[1]

[1]University of California, San Diego

This PLL meets NB-IoT specifications with the best fractional spur-power performance among state-of-the-art low-power single-supply PLLs while using a low-power class-D VCO with a small resistor, improving phase noise by 3dB and reducing power consumption by 25% without any area overhead. The VCO, working at 729-960 MHz, is powered by an on-chip DC-DC converter with 90% efficiency without degrading the spur performance of the PLL, which is -67.5dBc for reference and -66.3dBc for fractional spurs.

11:20 AM

3-4
A Compact Dual-Core 26.1-to-29.9GHz Coupled-CMOS LC-VCO with Implicit Common-Mode Resonance and FoM of –191 dBc/Hz at 10MHz

Amir Masnadi[1]; Mohammad Mahani[1]; Hossein Miri Lavasani[2]; Shahriar Mirabbasi[3]; Sudip Shekhar[3]; Rod Zavari[1]; Hormoz Djahanshahi[1]

[1]Microchip Technology; [2]Case Western Reserve University; [3]University of British Columbia

A compact dual-core, single-transformer, and low-power coupled-Class-C voltage-controlled oscillator is presented.The single transformer provides resonance at both differential and common modes, eliminating the need for an explicit inductor for the common-mode resonance.It is implemented vertically using two top metal layers, resulting in significant area saving compared to the state-of-the-art.The VCO consumes 3.4 mW at 27.45 GHz and exhibits a phase noise of –127.5 dBc/Hz at 10 MHz offset resulting in an FoM of −191 dB/Hz

Monday, March 23, 2020, 10:00 AM–12:00 PM

Session 4: Forum: Electronics for Vehicles of the Future

Sponsored by SiFive
Session Chair: Hanh-Phuc Le, University of California San Diego
Session Co-Chair: Dina El-Damak, USC

10:00 AM

4-1
Edge Computing and Resilient Hardware in Future Mobile and Autonomous Systems
Vijay Janapa Reddi, Harvard

10:30 AM

4-2
High-Performance Systems-on-Chip (SoCs) for ADAS
Adam Sherer, Cadence

11:00 AM

4-3
Electronics for Vehicles of the Future – Gate Drivers with Integrated Power Management
Sri Navaneeth Easwaran, Texas Instruments

11:30 AM

4-4
LIDAR Technology
Ron Kapusta, ADI

Monday, March 23, 2020, 10:00 AM–12:10 PM

Session 5: System Oriented Design Foundations

Session Chair: Mitsuhiko Igarashi, Renesas Electronics Corporation
Session Co-Chair: Luca Daniel, Massachusetts Institute of Technology

The session focuses on packaging technologies and design productivity solutions that enable large scale system development and integration.

10:00 AM

Introduction: System Oriented Design Foundations

10:05 AM Invited Paper

5-1
Multi-die Integration Using Advanced Packaging Technologies
Hyung-Jin Lee[1]; Ravi Mahajan[1]; Ramune Nagisetty[1]; Manish Deo[1]; Farhana Sheikh[1]
[1]Intel Corporation

This paper presents 2-D and 3-D multi-die integration technologies to create new types of system platforms that co-integrate multiple dies on package that may or may not be implemented in the same technology. The paper first presents challenges of process scaling and coexistence of logic, IO, and RF, and discusses new system/platform requirements from emerging applications.Then on-package 2-D/3-D multi-die integration technologies are presented. Finally, we present three innovative CPU and FPGA leveraging these technologies.

10:55 AM

5-2
A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process

Venkata Chaitanya Krishna Chekuri[1]; Nael Mizanur Rahman[1]; Edward Lee[1]; Arvind Singh[1]; Saibal Mukhopadhyay[1]

[1]Georgia Institute of Technology

This paper presents a fully synthesized integrated inductive buck regulator with flexible precision variable frequency feedback loop implemented in 65nm CMOS process using an automated design and GDSII generation flow. The design demonstrates 0.52V/us output ramp and 200ns response time to 30mA/75ps load transient in a high precision mode with 120MHz switching frequency, and peak efficiency of 79.3%.

11:20 AM Invited Paper

5-3
HL5: A 32-bit RISC-V Processor Designed with High-Level Synthesis

Paolo Mantovani[1]; Robert Margelli[1]; Davide Giri[1]; Luca Carloni[1]

[1]Department of Computer Science - Columbia University

We show that high-level synthesis (HLS) can simplify the design of processors while enhancing their customization and reusability. We present HL5 as the first 32-bit RISC-V microprocessor designed with SystemC and optimized with a commercial HLS tool. By describing the challenges and opportunities of applying HLS to processor design, our paper aims also at sparking a renewed interest in HLS research.

Monday, March 23, 2020, 08:30 AM–08:50 AM

Keynote Luncheon

12:00 PM

Microelectronics for Brain-Computer Interface Applications

Lawrence Larson, Sorensen Family Dean of the School of Engineering, Brown University

As integrated circuit technology becomes increasingly deployed to address the challenges of human health, the opportunity to interface directly to the brain is one of the most exciting and high impact

opportunities. Challenges like epilepsy, paraplegia, quadriplegia, locked-in syndrome, MLS, Parkinsons, and many others, are being addressed by this new technology. The recent announcement of significant advances by Neuralink is one example of the potential.This talk will summarize some of the challenges and opportunities of brain-computer-interface (BCI) technology from an integrated circuit perspective.

Bio: Larry Larson received his B.S. from Cornell University and his Ph.D. from UCLA. From 1980 to 1996, he was with Hughes Research Laboratories, Malibu, CA, USA, where he directed the development of high-frequency microelectronics in GaAs, InP, Si/SiGe, and MEMS technologies. In 1996, he joined the faculty of the University of California at San Diego (UCSD), where he was the inaugural holder of the Communications Industry Chair. From 2001 to 2006, he was Director of the UCSD Center for Wireless Communications, and from 2007 to 2011, was Chair of the Department of Electrical and Computer Engineering. In 2011, he joined Brown University, Providence, RI, USA, where he is Sorensen Family Dean of the School of Engineering. He has authored or coauthored over 300 papers and has coauthored four books. He holds over 40 U.S. patents.

Monday, March 23, 2020, 02:00 PM–05:15 PM

Session 6: Emerging Devices and Sensing Applications

Session Chair: Drew Hall, University of California San Diego
Session Co-Chair: Kiichi Nitsu, Nagoya University

This session covers emerging devices and sensing applications ranging from high performance thin film devices, their use in circuits and systems, and as biosensors. The first paper is an invited paper that reviews piezoelectric and ferroelectric devices with applications from filters and energy harvesters to ferroelectric memories. The second paper presents full-swing logic gates realized using only n-type a-Si:H thin film transistors demonstrated by implementing a decoder. The fourth paper presents an integrated readout circuit dedicated to sensing transcutaneous oxygen employing a fluorescence-based method to sense the oxygen molecules diffusing through the skin. The fifth paper presents a dual-factor authentication protocol based on detection of tap patterns for implantable medical device security. The last paper presents a highly-efficient and low-minimum input voltage energy harvester for bio-fuelcells with a cold startup enhancement technique.

02:00 PM

Introduction: Emerging Devices and Sensing Applications

02:05 PM Invited Paper

6-1
Doping of Aluminum Nitride and the Impact on Thin Film Piezoelectric and Ferroelectric Device Performance

Roy Olsson III[1]; Zichen Tang[1]; Michael D'Agati[1]
[1]University of Pennsylvania

Recently, the substitutional doping of scandium (Sc) for aluminum (Al) to form aluminum scandium nitride (AlScN) has been studied to enhance the piezoelectric properties and introduce ferroelectric properties into aluminum nitride (AlN) based material systems. This paper reviews the piezoelectric and ferroelectric performance that has been demonstrated, and the impact of the material properties on the performance

of piezoelectric and ferroelectric devices.

02:55 PM

6-2
Realization of an Energy-Efficient, Full-Swing Decoder with Unipolar TFT Technology

Qing Li[1]; Czang-Ho Lee[1]; William Wong[1]; Manoj Sachdev[1]
[1]University of Waterloo

Realization of full-swing logic gates is challenging using only one transistor type. Most such logic gates lack full-swing with excessive direct-path leakage current. Consequently, realization of multi-stage logic circuits becomes unrealistic. We propose novel logic gates without these problems. As a proof, we fabricated a 3-to-8 decoder with n-type a-Si:H TFTs. Measurement results demonstrated that the circuit could maintain unity stage-to-stage gain, while reduce 85% of static leakage current and 20% footprint against prior implementations.

03:20 PM **Best Regular Paper Candidate**

6-3
A Fully-Printed Organic Smart Temperature Sensor for Cold Chain Monitoring Applications

Marco Fattori[1]; Carlos Mendes da Costa[1]; Joost Fijn[1]; Enrico Genco[1]; Pieter Harpe[1]; Eugenio Cantatore[1]; Micael Charbonneau[2]
[1]Eindhoven University of Technology; [2]CEA-LITEN

This paper presents a smart temperature sensor on RFID suitable for fresh food monitoring. The system-on-foil exploits printed resistors and a time-based printed OTFT interface to convert temperature to a PWM representation and enable wireless RF communication at 13.56MHz. It achieves 270mKrms resolution for a 2s conversion time, a resolution FOM of 294μJ·K2 and a 3σ inaccuracy of ±1.2°C over the temperature range 3°C to 27°C, after systematic non linearity removal and 3-point calibration.

03:45 PM

Break

04:00 PM

6-4
An Integrated Readout Circuit for a Transcutaneous Oxygen Sensing Wearable Device

Ian Costanzo[1]; Devdip Sen[1]; Ulkuhan Guler[1]
[1]Worcester Polytechnic Institute

This paper presents an integrated readout dedicated to sensing transcutaneous oxygen, a first of its kind. The readout circuit employs a fluorescence-based methodto sense the oxygen molecules diffusing through the skin. The system uses a platinum porphyrin thin film, a blue light-emitting diode that excites

the thin film, and a photodiode that captures the red light emitted from the thin film. The paper presents the circuit design, oxygen measurement curve, and preliminary ex vivo testing.

04:25 PM

6-5
A Low-Power Dual-Factor Authentication Unit for Secure Implantable Devices

Saurav Maji[1]; Utsav Banerjee[1]; Samuel Fuller[1]; Samuel Fuller[2]; Mohamed Abdelhamid[1]; Phillip Nadeau[2]; Rabia Yazicigil[3]; Anantha Chandrakasan[1]
[1]Massachusetts Institute of Technology; [2]Analog Devices; [3]Boston University

This paper presents a dual-factor authentication protocol and its low-power implementation for security of implantable medical devices. The protocol incorporates user's touch based voluntary response in addition to cryptographic authentication. The wake-up unit of the test-chip consumes only 735pW of idle state power at 20.15Hz and 2.5V. The dual-factor authentication unit, accelerated in hardware, consumes only 8uW power at 660kHz and 0.87V. The prototype was also tested using in-vitro measurements.

04:50 PM Best Student Paper Candidate

6-6
A Fully-Integrated Biofuel-Cell-Based Energy Harvester with 86% Peak Efficiency and 0.25V Minimum Input Voltage Using Source-Adaptive MPPT

Arian Hashemi Talkhooncheh[1]; You Yu[1]; Abhinav Agarwal[1]; William Kuo[1]; Kuan-Chang (Xavier) Chen[1]; Minwo Wang[1]; Gudrun Hoskuldsdottir[1]; Wei Gao[1]; Azita Emami[1]
[1]California Institute of Technology

This paper presents a cold-starting energy harvester in 65nm CMOS with source degradation tracking and automatic MPPT. A power-efficient architecture is proposed to keep the internal circuitry operating at 0.4V while regulating the output voltage at 1V using switched-capacitor DC-DC converters and a hysteresis controller. Peak efficiency of 86% is achieved at 0.39V input voltage and 1.34μW of output power with 220nW of internal average power consumption. Integrated operation with lactate biofuel cells is demonstrated.

Monday, March 23, 2020, 02:00 PM–05:15 PM

Session 7: RF & mm-WAVE Circuits and Transceivers

Session Chair: Debopriyo Chowdhury, Broadcom
Session Co-Chair: Swaminathan Sankaran, Texas Instruments

This session presents state of the art research on RF and mm-wave circuits and transceivers. The session begins with a wideband, 12-bit I/Q interleaved direct digital RF modulator from 0.5-3GHz with 320 MHz modulation bandwidth. Moving up higher in frequency, the next paper presents a two-way current combining power amplifier for 28GHz wireless communication in 22nm SOI technology. This will be followed by a mixer first extremely wideband 43-97GHz receiver front-end for massive MIMO applications. We then move onto full transceivers - starting with a 6-8 GHz pulse based transceiver for ranging, followed by a in depth review of millimeter-wave CMOS phased-array transceivers for 5G NR applications. Moving up even higher in frequency,

the session ends with a 113GHz transceiver in 28nm CMOS supporting an 80Gbps wireless link.

02:00 PM

Introduction: RF & mm-WAVE Circuits and Transceivers

02:05 PM

7-1
A 0.5--3 GHz I/Q Interleaved Direct-Digital RF Modulator with up to 320 MHz Modulation Bandwidth in 40 nm CMOS

Yiyu Shen[1]; Rob Bootsman[1]; Morteza Alavi[1]; Leo de Vreede[1]
[1]Delft University of Technology

This paper presents a wideband, 12-bit I/Q interleaved direct-digital RF modulator (DDRM) realized in 40-nm CMOS technology. The proposed digital-intensive quadrature up-converter features a novel I/Q-mapping unit cell to boost RF power, in-band linearity, and out-of-band spectral purity. The modulator provides more than 14 dBm RF output power . When applying a 320-MHz 256-QAM signal at 2.4 GHz, the measured ACLR and EVM is better than -43dBc and -32dB, respectively, without applying any digital predistortion.

02:30 PM

7-2
A 28GHz Two-Way Current Combining Stacked-FET Power Amplifier in 22nm FD-SOI

Zhiwei Zong[1]; Zhiwei Zong[2]; Xinyan Tang[1]; Xinyan Tang[2]; Johan Nguyen[2]; Johan Nguyen[1]; Khaled Khalaf[3]; Giovanni Mangraviti[1]; Yao Liu[1]; Piet Wambacq[1]; Piet Wambacq[2]
[1]IMEC; [2]Vrije Universiteit Brussel; [3]Pharrowtech

We present a two-way current combining power amplifier (PA) for 28GHz wireless communication. To boost the saturated output power (PSAT) and maintain a high power-added efficiency (PAE), a differential 3 stacked transistors structure is used for the unit PA cell. Measurement results show that the PA achieves a power gain of 27dB and a PSAT of 21.7dBm with a maximum PAE of 27.1% at 28GHz. The output 1dB compression point (P1dB) is 19.1 dBm.

02:55 PM

7-3
Mixer-First Extremely Wideband 43-97 GHz RX Frontend with Broadband Quadrature Input Matching and Current Mode Transformer-Based Image Rejection for Massive MIMO Applications

Amr Ahmed[1]; Min-Yu Huang[1]; Hua Wang[1]
[1]Georgia Institute of Technology

This work presents an ultra-wideband mixer-first front-end that can cover mmWave communications bands in the frequency range 43-97 GHz. The front-end employs a mmWave 90 degree coupler as an input stage in order to achieve wideband matching and RF quadrature signal generation. Passive mixer

and multi-gated gm3-cancellation IF amplifiers used to achieve and maintain high linearity across the frequency range. Also, the frond-end implements a current mode image rejection using a transformer based IF coupler.

03:20 PM

7-4
A 6-8GHz Multichannel Reconfigurable Pulse-Based Transceiver with 3.5ns Processing Latency and 1cm Ranging Accuracy for Secure Wireless Connectivity

Haixin Song[1]; Woogeun Rhee[1]; Zhihua Wang[1]
[1]Institute of Microelectronics

This paper describes a communication/ranging pulse-based transceiver that enables physical-layer security against relay attack. A reconfigurable transceiver system with concatenation operation is designed by having PPM/PWM-based two-bit communication between the prover and the verifier, significantly reducing the processing latency of the prover. Multichannel transmission with enhanced spectral efficiency and link margin are realized with channel hopping and subband hopping methods. The transceiver achieves

03:45 PM

Break

04:00 PM **Best Invited Paper Candidate**

7-5
Millimeter-Wave CMOS Phased-Array Transceiver Supporting Dual-Polarized MIMO for 5G NR

Kenichi Okada[1]; Jian Pang[1]
[1]Tokyo Institute of Technology

In this presentation, a 28-GHz phased-array transceiver designed for the coming 5G NR will be introduced. A neutralized bidirectional technique with minimized chip area is employed for a low-cost system. The data rate is improved significantly with a 2x2 dual-polarization MIMO configuration. The talk concludes with a discussion on future directions of millimeter-wave wireless communication, based on Shannon and Friis equations.

04:50 PM

7-6
A Fully Integrated, Dual Channel, Flip Chip Packaged 113 GHz Transceiver in 28nm CMOS supporting an 80 Gb/s Wireless Link

Andrew Townley[1]; Nima Baniasadi[1]; Sashank Krishnamurthy[1]; Constantine Sideris[2]; Ali Hajimiri[3]; Elad Alon[1]; Ali Niknejad[1]
[1]University of California at Berkeley; [2]University of Southern California; [3]California Institute of Technology

In this paper, a mm-wave transceiver IC operating at 113GHz is demonstrated, achieving a single-

channel data rate of 80Gb/s. The transceiver achieves a high level of integration, including LO generation circuitry, a bits-to-RF TX DAC, and two transceiver channels for polarization diversity. The chip is flip-chip packaged onto a PCB with two orthogonally polarized antennas.

Monday, March 23, 2020, 02:00 PM–05:15 PM

Session 8: Analog Circuits and Systems

Session Chair: Jiangfeng Wu, Tongji University Shanghai China
Session Co-Chair: Ivan O'Connell, University College Cork

This session includes papers describing systems and circuits which open up new opportunities for analog design. They include an invited paper on cryo-CMOS circuits, systems for fingerprint recognition and voice activity detection, and circuits for rapid start-up of a crystal oscillator, high-accuracy on-chip frequency reference, and ripple reduction in an instrumentation amplifier. The papers in this session open up new opportunities for analog IC design. They describe systems for fingerprint recognition and voice activity detection and circuits for cryogenic operation, rapid crystal oscillator start up, high-accuracy on-chip frequency reference, and ripple reduction with chopping.

02:00 PM

Introduction: Analog Circuits and Systems

02:05 PM

8-1
A 368 × 184 Optical Under-Display Fingerprint Sensor With Global Shutter and High-Dynamic-Range Operation

Chih-Wen Lu[1]; Ping-Hung Yin[2]; Ping-Hung Yin[1]; Jia-Shyang Wang[2]; Keng-Li Chang[2]; Fu-Kuo Lin[2]; Chia-Jung Chang[2]; Gen-Chiuan Bai[2]
[1]National Tsing Hua University; [2]TYRAFOS Technologies Co., LTD

This study proposes a 368 × 184 optical under-display fingerprint sensor. The prototype sensor features low noise, low-power consumption, fast response time, and a smaller signal processing circuit area. A dynamic range of 120 dB is achieved with 8-segment auto exposure and dark level adjustment with programmable gain control. The sensor has a chip size of 9.74 mm × 4.6 mm, a resolution of 1154 dpi, and a sensing area of 73%.

02:30 PM Best Regular Paper Candidate

8-2
A 760nW, 180nm CMOS Analog Voice Activity Detection System

Marco Croce[1]; Brian Friend[2]; Francesco Nesta[2]; Lorenzo Crespi[2]; Piero Malcovati[1]; Andrea Baschirotto[3]
[1]University of Pavia; [2]Synaptics; [3]University of Milano-Bicocca

This paper presents an SNR based voice-activity detection circuit, which consumes 760nW, exploiting an energy-efficient analog implementation with continuous-time non-linear operation and fully-passive switched-capacitor processing..

02:55 PM Invited Paper

8-3
Cryo-CMOS for Analog/Mixed-Signal Circuits and Systems

Fabio Sebastiano[1]; Jeroen van Dijk[1]; Pascal 't Hart[1]; Gerd Kiene[1]; Ramon Overwater[1]; Pinakin Padalia[1]; Job van Staveren[1]; Masoud Babaie[1]; Andrei Vladimirescu[3]; Andrei Vladimirescu[2]; Edoardo Charbon[5]; Edoardo Charbon[4]; Edoardo Charbon[1]; Edoardo Charbon[6]

[1]Delft University of Technology; [3]Institut Supérieur d'Électronique de Paris; [2]University of California at Berkeley; [5]Intel corporation; [4]Kavli institute of nanoscience; [6]EPFL

CMOS circuits operating at cryogenic temperature (cryo-CMOS) are required in several low-temperature applications, e.g., in the cryogenic electronic interface for quantum processors. Such cryo-CMOS circuits must achieve extremely high performance while dissipating minimum power to be compatible with existing cryogenic refrigerators. This paper overviews the challenges and the opportunities in designing cryo-CMOS circuits, with a focus on analog and mixed-signal circuits, such as voltage references and data converters.

03:45 PM

Break

04:00 PM

8-4
An 11.1nJ-Start-up 16/20MHz Crystal Oscillator with Multi-Path Feedforward Negative Resistance Boosting and Optional Dynamic Pulse Width Injection

Xiaoyang Wang[1]; Patrick Mercier[1]

[1]University of California, San Diego

This paper presents a fast start-up crystal oscillator that reduces both start-up time and energy via an elegantly effective muti-path feedforward |Rn| boosting technique. To further improve start-up speed, yet with an imprecise on-chip ring oscillator, an optional dynamic pulse width injection is also proposed. The proposed fast start-up technique is implemented in 65nm process and tested with 20MHz and 16MHz crystals, achieve start-up times of 30µs and 34µs while consuming 11.1nJ and 13.2nJ, respectively.

04:25 PM

8-5
A Colpitts-Based Frequency Reference Achieving a Single-Trim ±120ppm Accuracy from -50 to 170°C

Alexander Delke[1]; Anne-Johan Annema[1]; Mark Oude Alink[1]; Yanyu Jin[2]; Jos Verlinden[2]; Bram Nauta[1]

[1]University of Twente; [2]NXP Semiconductors

A single-trim, high accuracy frequency reference is presented. The Colpitts LC-oscillator topology reduces the dependencies of the LC-tank quality factor on the oscillation frequency. With a fractional divider for frequency compensation it can serve as crystal-replacement. Measurements of the prototype (16 samples) in a 0.13µm high-voltage CMOS SOI process show ±120ppm accuracy from -50°C to 170°C. The oscillator dissipates 3.5mW from a 2.5V supply and has 220ppm/V supply-sensitivity without supply

regulation.

04:50 PM

8-6
A 13nV/√Hz 4.5μW Chopper Instrumentation Amplifier with Robust Ripple Reduction and Input Impedance Boosting Techniques

Liang Fang[1]; Ping Gui[1]
[1]Southern Methodist Univeristy

This paper presents a 13nV/√Hz, 4.5μW Capacitively-coupled Chopper IA. A three-terminal varactor structure is proposed to improve the linearity of conventional varactor by 20 times and implemented in positive feedback loop to boost the input impedance by 1000 times. An improved dynamic offset zeroing technique is also proposed to suppress chopping ripple to a mean of 300uV and a standard deviation of 500uV. This design achieves a NEF of 1.3 and a PEF of 1.1.

Monday, March 23, 2020, 02:00 PM–03:45 PM

Session 9: Forum: IP Blocks: Challenges for Next Decade Complex SoCs

Sponsored by SiFive
Session Chair: Elkim Roa, Universidad Industrial de Santander
Session Co-Chair: Carlos Tokunaga, Intel Corporation

02:00 PM

9-1
Hardware Specialization for Next-Generation Computer Vision SoCs
Paul Whatmough, Arm ML Research Lab

2:35 PM

9-2
Challenges and Solutions for Domain-Specific Custom Silicon
Shubu Mukherjee, SiFive

03:10 PM

9-3
Data Converter IPs for Next-Generation Automotive Radar and LiDAR SoCs
Denis Daly, Omni Design Technologies, Inc.

Tuesday, March 24

Tuesday, March 24, 2020, 09:00 AM–11:35 AM

Session 12: Data Converter Techniques

Session Chair: Filip Tavernier, KU Leuven
Session Co-Chair: Gil Engel, Analog Devices

The popularity of SAR ADCs keeps increasing thanks to its beneficial scaling trends. This is clearly highlighted in the first four papers in this session on advanced data converter techniques including a pipelined SAR ADC with a novel amplifier settling time enhancement, a ring-amplifier based pipelined SAR with dynamic deadzone control to enable an ultra-low supply voltage of 0.75 V, a secure SAR ADC utilizing current equalization to prevent power side-channel attacks and a 0.2 V supply SAR ADC utilizing clever comparator techniques. The last paper is an invited submission describing digital correction of DAC non-linearities in multi-bit feedback ADCs.

09:00 AM

Introduction: Data Converter Techniques

09:05 AM

12-1
A 1.5GS/s 8b Pipelined-SAR ADC with Output Level Shifting Settling Technique in 14nm CMOS

Yuanming Zhu[1]; Shengchang Cai[1]; Shiva Kiran[1]; Yanghang Fan[1]; Pohsuan Chang[1]; Sebastian Hoyos[1]; Samuel Palermo[1]
[1]Department of Electrical and Computer Engineering, Texas A&M University

A single channel 1.5GS/s 8-bit pipelined-SAR ADC utilizes a novel correlated level shifting (CLS) settling technique to reduce the power and enable low-voltage operation of the dynamic residue amplifier. Fabricated in a 14nm FinFET technology, the ADC occupies 0.0013mm2 core area and operates with a 0.8V supply. 6.6-bit ENOB is achieved at Nyquist while consuming 2.4mW, resulting in an FOM of 16.7fJ/conv.-step.

09:30 AM

12-2

A 72.6 dB SNDR 14b 100 MSPS Ring Amplifier Based Pipelined SAR ADC with Dynamic Deadzone Control in 16 nm CMOS

Martin Kinyua[1]; Eric Soenen[1]
[1]TSMC

This work presents a ring amplifier based pipelined SAR ADC. It employs a dynamic deadzone control circuit in the second stage inverter structure of a three stage amplifier, enhancing stability and enabling operation at ultra-low supply voltage of 0.75V. A 14 bit 100 MSPS prototype in 16nm consumes 2.5 mW and achieves SNDR and SFDR of 72.6dB and 86.5dB respectively, close to Nyquist input frequency, yielding a SNDR based FOM of 175.6dB without calibration

09:55 AM

12-3
S2ADC: A 12-bit, 1.25MS/s Secure SAR ADC with Power Side-Channel Attack Resistance

Taehoon Jeong[1]; Anantha Chandrakasan[1]; Hae-Seung Lee[1]
[1]Massachusetts Institute of Technology

An ADC in sensing hardware can create a critical security loophole by revealing private sensor data through its power side-channel. This paper demonstrates a neural-network-based SAR ADC power side-channel attack (PSA) method that can extract A/D conversion results from ADC supply current waveforms with high accuracy and a current-equalizer-based PSA protection scheme that protects all ADC blocks from the proposed PSA method.

10:20 AM

12-4
A 0.2-V 10-bit 5-kHz SAR ADC with Dynamic Bulk Biasing and Ultra-Low-Supply-Voltage Comparator

Alexander Petrie[1]; Whitney Kinnison[1]; Yixin Song[1]; Kent Layton[2]; Shiuh-hua Wood Chiang[1]
[1]Brigham Young University; [2]ON Semiconductor

A 10-bit 5-kHz SAR ADC under an ultra-low-supply-voltage of 0.2 V demonstrates a novel dynamic bulk biasing circuit to tolerate variations. A new comparator relaxes the stringent speed-noise trade-off under the 0.2-V supply. The measured ADC consumes 22 nW and exhibits an SNDR of 52.8 dB, yielding an FoM of 12.3 fJ/conv.-step. Measurements of multiple chips show the proposed dynamic bulk biasing successfully improves the yield by nearly twofold in the presence of supply variations.

10:45 AM Invited Paper

12-5
Digital Correction of DAC Nonlinearity in Multi-Bit Feedback A/D Converters

Pedram Payandehnia[1]; Tao He[1]; Yanchao Wang[1]; Gabor Temes[1]
[1]School of Electrical Engineering and Computer Science, Oregon State University

In this paper, an overview of existing methods for correcting or mitigating the effects of DAC imperfections is presented. Also, a new foreground digital correction method is described for the mitigation of static mismatch errors in the binary-weighted DAC.

Tuesday, March 24, 2020, 09:00 AM–11:10 AM

Session 13: Efficient Neural Network Acceleration

Session Chair: Brian Zimmer, Nvidia
Session Co-Chair: Greg Chen, Intel Corporation

This session explores a wide variety of techniques to improve the energy efficiency of neural network computation, with the first two papers focusing on compute-in-memory approaches and the last two papers optimizing conventional digital techniques. The first paper surveys state-of-the-art compute-in-memory prototypes, while the second paper uses a compute-in-memory approach for keyword spotting acceleration. The third paper improves energy efficiency through variable-precision computation, and the last paper avoids redundant computation with zero skipping and reduced-precision pooling prediction.

09:00 AM

Introduction: Efficient Neural Network Acceleration

09:05 AM Invited Paper

13-1
Compute-in-Memory with Emerging Nonvolatile-Memories: Challenges and Prospects

Shimeng Yu[1]; Xiaoyu Sun[1]; Xiaochen Peng[1]; Shanshi Huang[1]
[1]Georgia Institute of Technology

This invited paper surveys the recent progresses of compute-in-memory (CIM) prototype chip designs with emerging nonvolatile memories (eNVMs) such as resistive random access memory (RRAM) technology. However, grand challenges exist for large-scale system design including the following: 1) substantial analog-to-digital (ADC) overhead; 2) scalability to advanced logic node limited by high write voltage of eNVMs; 3) process variations (e.g. ADC offset) that degrade the inference accuracy. Mitigation strategies and possible future research directions are discussed.

09:55 AM

13-2
KeyRAM: A 0.34 uJ/decision 18 k decisions/s Recurrent Attention In-memory Processor for Keyword Spotting

Hassan Dbouk[1]; Sujan Gonugondla[1]; Charbel Sakr[1]; Naresh Shanbhag[1]
[1]University of Illinois at Urbana-Champaign

This paper presents a 0.34uJ/decision deep learning-based classifier for keyword spotting (KWS) in 65nm CMOS with all weights on-chip. This work adapts a Recurrent Attention Model algorithm for the KWS, and employs an in-memory computing (IMC) architecture to achieve up to 9× savings in energy/decision and >23× savings in EDP of decisions over a state-of-the art IMC IC for KWS using the Google Speech dataset while achieving the highest reported decision throughput of 18.32k decisions/s

10:20 AM

13-3
A 44.1TOPS/W Precision-Scalable Hardware Accelerator for Quantized Neural Networks in 28nm CMOS

Sungju Ryu[1]; Hyungjun Kim[1]; Wooseok Yi[1]; Jongeun Koo[1]; Eunhwan Kim[1]; Yulhwa Kim[1]; Taesu Kim[1]; Jae-Joon Kim[1]

[1]Pohang University of Science and Technology

Quantized neural networks have been introduced to reduce computation time and energy when performing neural network algorithms. However, in the precision-scalable hardware, bit-reconfiguration logic significantly increases chip area. In this paper, we introduce a compact precision-scalable hardware accelerator. We improved peak performance per compute area by 5.1-7.7x and system-level energy-efficiency by 28-64% compared to previous precision-scalable accelerators.

10:45 AM

13-4
Deep Convolutional Neural Network Accelerator Featuring Conditional Computing and Low External Memory Access

Minkyu Kim[1]; Jae-sun Seo[1]

[1]Arizona State University

This paper presents an ASIC accelerator for deep convolutional neural networks (DCNNs) featuring a novel conditional computing scheme that synergistically combines precision-cascading (PC) with full zero-skipping (ZS). By jointly optimizing the proposed algorithm and the hardware architecture, the prototype chip implemented in 40nm CMOS demonstrates a peak energy-efficiency of 8.88 TOPS/W at 0.9V supply and low external memory access of 55.31MB (or 0.0018 access/MAC) for ImageNet classification with VGG-16 CNN.

Tuesday, March 24, 2020, 09:00 AM–11:35 AM

Session 14: DC-DC Converters

Session Chair: Yan Lu, University of Macau
Session Co-Chair: Eric Soenen, TSMC

This session includes four original designs of DC-DC converters, as well as one invited review paper on ultra-low-power energy harvesting power management circuit design. The session starts with a Buck converter with a fast response active ramping voltage mode control scheme, followed by three papers on highly-integrated hybrid multilevel or multiple-output DC-DC converters achieving high efficiencies, fast responses, and small ripples/cross-talks. Last but not least, we dive into micro- or even pico-Watts-level power management units for IoT devices, focusing on the choice between analog and digital implementations.

09:00 AM

Introduction: DC-DC Converters

09:05 AM

14-1

A 9.3mV / 5.2mV Load and Line Transients Fast Response Buck Converter with Active Ramping Voltage Mode Control

Wanyuan Qu[1]; Xu Yang[1]; Haixiao Cao[1]
[1]Institute of VLSI Design School of ISEE, Zhejiang University

A fast response active ramping voltage mode control scheme for a Buck converter design is presented. Analysis and measurements indicate that the scheme shows performance comparable to ripple-based controls while maintaining fixed frequency operation. Measurements show an under-/overshoot voltage of -12.7 mV and 9.3 mV, respectively, for load transitions between 100 mA and 500 mA. The line transient is 5.2 mV and -3.8 mV, respectively, for inputs between 12 V and 15 V.

09:30 AM

14-2
A 92.4% Efficient, 5.5V:0.4-1.2V, FCML Converter with Modified Ripple Injection Control for Fast Transient Response and Capacitor Balancing

Jan Rentmeister[1]; Jason Stauth[1]
[1]Dartmouth College

This paper presents a highly-integrated, 5-level flying capacitor multilevel (FCML) DC-DC converter that uses augmented ripple-injection control to achieve fast transient response and flying capacitor voltage balance. The converter provides 5.5V:0.4-1.2V step down with robust load- and line-rejection, and peak efficiency of 92.4% and >80% efficiency at a 13.8:1 conversion ratio with peak current up to 1.4A.All power devices, bootstrap capacitors, and control functions are integrated on-chip; capacitors are die-attached using a custom assembly process.

09:55 AM

14-3
A Wide Output Voltage Range Single-Input-Multi-Output Hybrid DC-DC Converter Achieving 87.5% Peak Efficiency With a Fast Response Time and Low Cross Regulation for DVFS Applications

Zhiyuan Zhou[1]; Nghia Tang[1]; Bai Nguyen[1]; Wookpyo Hong[1]; Partha Pande[1]; Deukhyoun Heo[1]
[1]Washington State University

A SIMO hybrid converter is presented, which obtains fast response, low cross-regulation, and high efficiency by using a multi-output hybrid power stage and a dual-switching-frequency technique. The hybrid power stage improves efficiency without sacrificing the output voltage range, and the dual-switching-frequency technique enhances the response and cross-regulation.The converter achieves 87.5% peak efficiency with output voltage range from 0.4V to 1.6V, it also achieves less than 0.01mA/mV

cross-regulation and less than 20mV overshoot during transient response.

10:20 AM

14-4
H-SIMO: A Hybrid Single-Inductor Multi-Output Thin-Oxide Power Management Unit Achieving 91.4% Efficiency from Li-ion Battery Voltages in 28nm FD-SOI

Sally Amin[2]; Sally Amin[1]; Patrick Mercier[1]
[2]Intel Corporation; [1]University of California San Diego

This paper presents a miniaturized Li-ion-compatible hybrid single-inductor multi-output(H-SIMO) power management unit (PMU) in 28nm FD-SOI for powering IoT devices.Miniaturization is achieved by combining the benefits of SIMO converters with the benefits of hybrid-multi-level converters. The PMU is implemented in an arrangement that naturally exploits the required transistor stacking to enable coverage of the 2.8-4.2V Li-ion-battery-voltage using only 1V-thin-oxide transistors.The fabricated die independently regulates 3 outputs over 0.4-0.9V from 10uW-40mW using 1.28mm^3-inductor with 91.4% peak-efficiency.

10:45 AM Invited Paper

14-5
Sub-microAmp Energy Harvesting and Power Management Units for Self-Powered IoT SoCs: Analog vs. Digital Implementations (Invited)

Shuo Li[1]; Benton Calhoun[1]
[1]University of Virginia

This paper reviews the design trends and techniques for sub-microamp EH-PMUs. Analyzing the power trend of IoT components shows the load power is reducing from µW to pW level, which requires that EH-PMUs have sub-µA quiescent current to power those loads efficiently. ULP techniques are reviewed with three examples focusing on analog vs. digital implementations, an MIMO EH-PMU with analog vs. digital ZCDs, ALDO vs. DLDO, and an analog MPPT algorithm for piezoelectric energy harvesting.

Tuesday, March 24, 2020, 11:35 AM–01:30 PM

Lunch Break

Tuesday, March 24, 2020, 01:30 PM–05:35 PM

Session 16: Energy-Efficient Systems for Wearable, Implantable, and IoT Applications

Session Chair: Mahsa Shoaran, Cornell University
Session Co-Chair: Ulkuhan Guler, Worcester Polytechnic Institute

This session features emerging low-power systems for wearable/implantable and IoT technologies, with topics ranging from neural interfaces to low-power light sensors and machine learning hardware for biomedical applications.

01:30 PM

Introduction: Energy-Efficient Systems for Wearable, Implantable, and IoT Applications

01:35 PM

16-1
A Fully-integrated Gesture and Gait Processing SoC for Rehabilitation with ADC-less Mixed-signal Feature Extraction and Deep Neural Network with Online Training

Yijie Wei[1]; Kofi Otseidu[2]; Qiankai Cao[1]; Levi Hargrove[3]; Jie Gu[1]
[1]Northwestern University; [2]Intel; [3]Shirley Ryan AbilityLab

An ultra-low-power gesture and gait classification SoC is presented for rehabilitation application featuring (1) mixed-signal feature extraction and integrated low-noise amplifier eliminating expensive ADC and digital feature extraction, (2) an integrated distributed deep neural network (DNN) ASIC supporting a scalable multi-chip neural network for sensor fusion with distortion resiliency for low-cost front end modules, (3) on-chip learning of DNN engine allowing in-situ training of user-specific operations.

02:00 PM

16-2
A 9.6 mW/Ch 10 MHz Wide-bandwidth Electrical Impedance Tomography IC with Accurate Phase Compensation for Breast Cancer Detection

Jaehyuk Lee[1]; Surin Gweon[1]; Kwonjoon Lee[1]; Soyeon Um[1]; Kyoung-rog Lee[1]; Kwantae Kim[1]; Jihee Lee[1]; Hoi-Jun Yoo[1]
[1]Korea Advanced Institute of Science and Technology (KAIST)

In this paper, we propose an 8-channel 10 MHz wide-bandwidth EIT AFE IC for compact and accurate breast cancer detection system. Thanks to the key features, the proposed prototype breast cancer detection system with the dedicated EIT IC can operate up to 10MHz with a small phase error of 4.32 degree, eventually can detect a small size target object of 0.5 cm and verified with the phantom experiments.

02:25 PM

16-3
A 43.8μW per Channel Biopotential Readout System using Frequency Division Multiplexing with Cable Motion Artifact Suppression

Jinyong Kim[1]; Hyunkyu Ouh[1]; Matthew Johnston[1]
[1]Oregon State University

This paper presents a fully-integrated biopotential readout system using frequency division multiplexing (FDM) for general purpose, multi-channel bipotential signal acquisition. FDM reduces the number of required cables between active electrode and back-end readout, and frequency translation prior to transmission mitigates low-frequency motion artifacts and mains interference in the cable. A 4-channel

EMG/ECG architecture was fabricated in 180nm CMOS and consumes only 43.8uW per channel, and measured results include demonstrated EMG and ECG applications.

02:50 PM

16-4
A 151nW Second-Order Ternary Delta Modulator for ECG Slope Variation Measurement with Baseline Wandering Resilience

Xiaochen Tang[1]; Wei Tang[1]
[1]New Mexico State University

This paper presents a second-order ternary delta modulator for ECG delineation. The proposed circuit measures the slope variation of the ECG signals to detect the turning points. Thus fiducial points of the PQRST waves can be located for on-chip arrhythmia classification. The chip achieves 3 ms timing error and shows robustness to baseline wandering. The circuit consumes 151 nW with 1 V supply at a sampling rate of 1 kS/s.

03:15 PM

Break

03:30 PM Invited Paper

16-5
Design and Optimization of Low Power and Low Light Sensors

Christian Enz[1]; Assim Boukhayma[1]; Antonino Caizzone[1]; Raffaele Capoccia[1]
[1]EPFL ICLAB

This paper shows that many low-light applications share the same readout architecture. It explains how the readout circuit can be optimized for reaching a minimum input-referred noise without penly on the power consumption. The design methodology is then illustrated by three applications, including a 0.5 electrons rms CMOS VGA imager, a 2.6uW PPG sensor and a 10uW 1D time-of-flight distance ranging device.

04:20 PM

16-6
A 12.5mg mm-Scale Inductively-Powered Light-Directivity-Enhanced Highly-Linear Bidirectional Optogenetic Neuro-Stimulator

Tayebeh Yousefi[1]; Mansour Taghadosi[1]; Alireza Dabbaghian[1]; Ryan Siu[1]; Gerd Grau[1]; Georg Zoidl[1]; Hossein Kassiri[1]
[1]York University

A mm-scale self-contained bidirectional optogenetic stimulator is presented. A novel LED driving circuit is employed allowing for fully-linear control of optical stimulation with the smallest reported 200mV headroom, significantly boosting the electrical-to-optical energy-conversion efficiency. The energy efficiency is further improved (30.46x) by custom-designed light-directivity-enhancing printed ulenses. In addition to the two stimulation channels, the SoC integrates two recording channels (Gain=48.3dB,IIRN=5.29uVRMS,SNDR=45.15dB) and is powered through an on-chip coil. Electrical,

optical, and in-vitro measurement results are reported.

04:45 PM

16-7
A 10.13uJ/classification 2-channel Deep Neural Network-based SoC for Emotion Detection of Autistic Children

Muhammad Awais Bin Altaf[1]; Abdul Rehman Aslam[1]; Hafiz Talha Iqbal[1]; Mahnoor Aftab[1]; Wala Saadeh[1]

[1]Lahore University of Management Sciences

An EEG-based noninvasive neuro-feedback SoC for emotion classification of Autistic children is presented. The AFE comprises two entirely shared EEG-channels using sampling capacitors to reduce the area by 30% and achieve an overall integrated input-referred noise of 0.55µVRMS with cross-talk of -79dB. The 4-layers Deep Neural Network (DNN) classifier is integrated on-sensor to classify (4 emotions) with >85% accuracy. The 16mm2 SoC in 0.18um CMOS consumes 10.13µJ/classification for 2 channels.

05:10 PM

16-8
A 27Mbps, 0.08mm^3 CMOS Transceiver with Simultaneous Near-field Power Transmission and Data Telemetry for Implantable Systems

Jordan Thimot[1]; Kukjoo Kim[1]; Chen Shi[1]; Kenneth Shepard[1]

[1]Columbia University

This paper presents an inductively powered 27Mbps 0.08mm^3 CMOS transceiver with integrated RF receiver coils for simultaneous two-way, near-field data telemetry and power transmission for implantable systems. A four-coil inductive link operates with a 27MHz carrier for power and 700MHz carrier for uplink (27Mbps) and downlink (6.6kbps). Complete transceiver functionality of the system has been achieved with overall power transfer efficiency (PTE) of 1.04% through 1mm of tissue phantom between reader and implant.

Tuesday, March 24, 2020, 01:30 PM–05:10 PM

Session 17: SoC Design: From Bits to Gigabits

Session Chair: Saad Bin Nasir, Qualcomm
Session Co-Chair: Nachiket Desai, Intel
Session Co-Chair: Xuanyao Fong, National University of Singapore

This session covers advances in SoCs spanning from full systems, to accelerators, to fundamental building blocks. The first paper addresses advances in digital control of integrated voltage regulars. The next two SoCs optimize performance across runtime conditions by monitoring temperature/power or communication channel conditions. The fourth paper highlights power management in a RISC-V microcontroller that performs periodical sensing. This is followed by a building block paper which shows a differential low-power flop design. The final two papers show accelerator blocks for genome sequencing and compressed sensing-based radar.

01:30 PM

Introduction: SoC Design: From Bits to Gigabits

01:35 PM

17-1
Randomized Pulse-Modulating Instruction-Issue Control Circuit for a Current and Temperature Limiting System in a 7nm Hexagon™ Compute DSP

Vijay Kiran Kalyanam[1]; Eric Mahurin[1]; Keith Bowman[2]; Jacob Abraham[3]
[1]Qualcomm Technologies,Inc.; [2]Qualcomm Technologies Inc.; [3]University Texas at Austin

We describe a randomized pulse-modulation (RPM) circuit for controlling the instruction-issue rate in a Qualcomm® Hexagon™ compute multi-threaded compute DSP (CDSP) for adapting performance to limit current and temperature below target thresholds. Silicon measurements from a 7nm CDSP demonstrate that the RPM adjusts performance in ~5 CDSP clock cycles after synchronization and enables 0.4% performance resolution across a wide range of operation while avoiding thread-starvation and satisfy the 1 micro-sec latency requirement for the entire limiting system.

02:00 PM

17-2
A 41.5 pJ/b, 2.4GHz Digital-Friendly Orthogonally Tunable Transceiver SoC with 3-decades of Energy-Performance Scalability

Baibhab Chatterjee[1]; Shreyas Sen[1]
[1]Purdue University

In this paper, we present a digital-friendly Transceiver SoC consisting of an RF-DAC based transmitter with orthogonally tunable output power, data rate and ECC that enables optimum system level bit error rate (BER) and energy for over 3-orders of energy-performance scalability, along with an ultra-low-power OOK receiver that receives the transmitter's control bits from a nearby base station for closed-loop control.

02:25 PM Invited Paper

17-3
Digital Control of Switching and Linear Integrated Voltage Regulators

Harish Krishnamurthy[1]; Zakir Ahmed[1]; Xiaosen Liu[1]; Nachiket Desai[1]; Suhwan Kim[1]; Nicolas Butzen[1]; Sally Amin[1]; Sheldon Weng[1]; Krishnan Ravichandran[1]; James Tschanz[1]; Vivek De[1]
[1]Intel Labs

This work presents a summary of the digital control techniques in todays IVRs and the role digital control is playing to enhance their key performance metrics. Examples from high switching frequency Buck converters, computationally controlled digital LDOs as well as hybrid LDOs speaks not only to the growing popularity of digital control in a wide variety of applications but also demonstrates its suitability on advanced process nodes which is inherently tough on analog circuits.

03:15 PM

Break

03:30 PM

17-4

An Energy-Efficient RISC-V RV32IMAC Microcontroller for Periodical-Driven Sensing Applications

Ckristian Duran[1]; Megan Wachs[2]; Luis Rueda[1]; Albert Huntington[2]; Hector Gomez[1]; Javier Ardila[1]; Andres Amaya[1]; Krste Asanovic[3]; Krste Asanovic[2]; Elkim Roa[1]

[1]OnChip - Universidad Industrial de Santander; [2]SiFive Inc.; [3]University of California at Berkeley

Reported work on minimum-energy (ME) computing for low-power applications has focused entirely on tracking solely the microprocessor ME voltage supply. However, the use of low-power systems requires accounting for regulator losses, voltage monitors, biasing, peripheral, clock sources, and start-up energies to adapt the correct ME supply to different operation modes. Here we demonstrate a 32-bit RISC-V IMAC based microcontroller in 180nm CMOS featuring a low-energy always-on (AON) subsystem extending on ME adaption by including peripherals.

03:55 PM

17-5

A Static Contention-Free Differential Flip-Flop in 28nm for Low-Voltage, Low-Power Applications

Gicheol Shin[1]; Eunyoung Lee[1]; Jongmin Lee[1]; Yongmin Lee[1]; Yoonmyung Lee[1]

[1]Sungkyunkwan University

A Static Contention-free Differential Flip-Flop (SCDFF) is presented in 28nm, targeting wide-range voltage scalability (1V to 0.3V). The SCDFF offers fully static and contention-free operation without redundant clock toggling with footed differential latches, while keeping same area with conventional transmission-gate flip-flop (TGFF). Measured power is reduced by 64%/56% with 0%/10% activity at 1V, compared to the TGFF, and 100 dies from 5 corners were functional down to 0.28V.

04:20 PM

17-6

A 2.46M reads/s Genome Sequencing Accelerator using a 625 Processing-Element Array

Zhehong Wang[1]; Tianjun Zhang[1]; Daichi Fujiki[1]; Arun Subramaniyan[1]; Xiao Wu[1]; Makoto Yasuda[2]; Satoru Miyoshi[3]; Masaru Kawaminami[2]; Masaru Kawaminami[3]; Reetuparna Das[1]; Satish Narayanasamy[1]; David Blaauw[1]

[1]University of Michigan; [2]Mie Fujitsu Semiconductor Limited; [3]Fujitsu Electronics America, Inc.

We present an accelerator for seed-extension, a critical and computational intensive step in genome sequencing. The accelerator consists of a triangular array of 25x25 custom design processing elements implementing a string-independent automata. It achieves 2.46M read/s, a ~1800x performance improvement, and 27x smaller silicon footprint compared to a Xeon E5420.

04:45 PM Best Student Paper Candidate

17-7
A 17.8MS/s Neural-Network Compressed Sensing Radar Processor in 16nm FinFET CMOS

Peter Brown[1]; Matthew O'Shaughnessy[2]; Christopher Rozell[2]; Justin Romberg[2]; Michael Flynn[1]
[1]University of Michigan; [2]Georgia Institute of Technology

Transceiver bandwidth limits the resolution of ultra-low-power pulse radar systems. Compressed sensing techniques improve resolution but existing efforts require heavy computation. This work proposes a neural-network based compressed sensing radar processor architecture that improves resolution by 6x while remaining computationally efficient. Fabricated in 16nm FinFET CMOS, the processor simultaneously achieves more than 8x throughput and 18x efficiency over the state-of-the-art.

Tuesday, March 24, 2020, 01:30 PM–03:15 PM

Session 18: Ultra-low Power Wireless Transceivers

Session Chair: Hossein Lavasani, Case Western Reserve University Industry
Session Co-Chair: Chris Rudell, University of Washington

The trend towards zero power radios for implantable systems and IoT continues to attract attention. This session will introduce several techniques for ultra-low power, short-range communication. An invited paper which opens this session presents a general overview of state-of-the-art low power communication receivers. The session continues with an ultra-wideband wirelessly powered implantable receiver which reports up to 150Mbps data rate and a 4.7pJ/b energy efficiency in TX mode and 1pJ/b while in the receive mode. The session will conclude with a paper which employs a high-Q MEMS filter to improve the sensitivity of an ultra-low power wakeup and data receiver to -108dbm.

01:30 PM

Introduction: Ultra-low Power Wireless Transceivers

01:35 PM Best Invited Paper Candidate

18-1
Ultra-Low Power Receivers for IoT Applications: A Review

David Wentzloff[1]; Abdullah Alghaihab[1]; Jaeho Im[1]
[1]University of Michigan

Efficient wireless connectivity is an important requirement for IoT applications and has attracted a lot of research interest recently. The receivers designed for such applications need to be low power while still supporting sufficient communication range and co-existing with other receivers that share the same frequency band. In addition, supporting adopted communication standards is key for ubiquitous integration with the existing infrastructure.

02:25 PM

18-2
A 1.6mm3 Wirelessly Powered Reconfigurable FDD Radio with On-Chip Antennas Achieving 4.7 pJ/b TX and 1 pJ/b RX Energy Efficiencies for Medical Implants

Hamed Rahmani[1]; Aydin Babakhani[1]
[1]University of California, Los Angeles

We present an integrated wirelessly powered radio with two on-chip antennas and a total volume of 1.6mm3. Power and DL data are carried to the system via an AKS-modulated RF link with an efficiency of 1pJ/p. The TX block, based on a power-oscillator, utilizes an on-chip dipole antenna at the load. Reconfigurable TX transmits UL data with OOK/UWB modulation schemes and archives a maximum data-rate of 150Mbps with an efficiency of 4.65pJ/b at 15cm distance.

02:50 PM

18-3
A -108dBm Sensitivity, -28dB SIR, 130nW to 41µW, Digitally Reconfigurable Bit-Level Duty-Cycled Wakeup and Data Receiver

Anjana Dissanayake[1]; Jesse Moody[1]; Henry Bishop[1]; Daniel Truesdell[1]; Henry Muhlbauer[1]; Ruochen Lu[2]; Anming Gao[2]; Songbin Gong[2]; Benton Calhoun[1]; Steven Bowers[1]
[1]University of Virginia; [2]University of Illinois Urbana-Champaign

A -108dBm, 430MHz highly digitally reconfigurable wake-up and data receiver in 65nmCMOS is presented. 2-tone OOK modulation and AlN-MEMS resonator enable an SIR of -28dB at 0.7% freq. offset from carrier. Configurable dynamic ranges of 11dB, 410X, 672X are achieved for sensitivity, power, and latency. In data Rx mode, 4.2kbps bit-rate at -108dBm sensitivity is achieved at 41uW. The WuRx is a highly digitally reconfigurable and interference robust candidate for emerging ultra-long-range IoT LPWAN.

Tuesday, March 24, 2020, 01:30 PM–02:50 PM

Session 19: Forum: Journey of a Startup

Sponsored by SiFive
Session Chair: Gregory Chen, Intel Corporation
Session Co-Chari: Carlos Tokunaga, Intel Corporation

01:30 PM

19-1
A Venture Capitalist's View of the Journey of a Start-Up
Jennifer Ard, Intel Capital

01:55 PM

19-2
Accelerating Artificial Intelligence with Light
Darius Bunandar, Chief Scientist, Lightmatter

02:20 PM

19-3
Self Powered Wireless Sensors for the Industrial Internet of Things: From Academic Projects to Full Solution Products
Benton Calhoun, Co-Founder & Co-CTO, Everactive

02:45 PM

19-4
Sifive: A Startup with a Mission to Democratize Access to Custom Cores and Silicon
Krste Asanovic, Co-Founder and Chief Architect, SiFive

Tuesday, March 24, 2020, 03:30 PM–05:40 PM

Session 20: High-Speed Wireline Transceivers

Session Chair: Tod Dickson, IBM T.J. Watson
Session Co-Chair: Kumar Lakshmikumar, Cisco Systems

This session highlights innovations in high-speed wireline transceivers for electrical interconnects, ranging from novel CDR and DFE techniques to architectures for state-of-the-art SerDes.

03:30 PM

Introduction: High-Speed Wireline Transceivers

03:35 PM Invited Paper

20-1
Short-Reach and Pin-Efficient Interfaces Using Correlated NRZ

Armin Tajalli[1]; Armin Tajalli[2]; Amin Shokrollahi[1]; Mani Bastai Parizi[1]; Dario Albino Carnelli[1]; Chen Cao[1]; Kiarash Gharibdoust[1]; Amit Gupta[1]; Ahmed Hassanin[1]; Klaas Hofstra[1]; Brian Holden[1]; Ali Hormati[1]; John Keay[1]; David Stauffer[1]; Richard Simpson[1]; Andrew Stewart[1]; Giuseppe Surace[1]; Omid Talebi Amiri[1]; Anton Tschank[1]; Roger Ulrich[1]; Christoph Walter[1]
[1]Kandou Bus; [2]University of Utah

Correlated Non-Return-to-Zero (CNRZ) signaling exhibits better pin-efficiency compared to the conventional binary differential NRZ signaling, while it does not compromise the sensitivity to Inter-Symbol Interference (ISI). This article analyzes performance of CNRZ transceivers, and provides experimental data for an Ultra-Short Reach (USR) link 20.83 Gb/s/wire, implemented in FinFET 16nm technology, and consuming 1.02 pJ/b.

04:25 PM

20-2
A 60-Gb/s PAM4 Wireline Receiver with 2-Tap Direct Decision Feedback Equalization Employing Track-and-Regenerate Slicers in 28-nm CMOS

Kuan-Chang Chen[1]; William Kuo[1]; Azita Emami[1]
[1]California Institute of Technology

A track-and-regenerate CMOS slicer is proposed and employed in a PAM4 receiver. The reduced delay of the slicer and its full-swing outputs allow a 2-tap direct decision-feedback equalizer at 60-Gb/s with improved energy efficiency and area requirements. Fabricated in 28-nm CMOS technology, the PAM4 receiver achieved BER better than 1E-12 at 60-Gb/s with 1.1pJ/b energy efficiency measured over a channel of 8.2dB loss at Nyquist rate.

04:50 PM

20-3
A 0.0285mm2 0.68pJ/bit Single-Loop Full-Rate Bang-Bang CDR without Reference and Separate Frequency Detector Achieving an 8.2(Gb/s)/µs Acquisition Speed of PAM-4 data in 28nm CMOS

Yong Chen[1]; Xiaoteng Zhao[1]; Pui-In Mak[1]; Rui P. Martins[1]
[1]University of Macau

To our knowledge this work is the first bang-bang CDR for PAM-4 signaling without reference and separate FD, while being more energy (>3.3x) and area (>1.6x) efficiencies than the prior art that support only NRZ signaling. The frequency acquisition is fully automatic, and the achieved acquisition speed of 8.2(Gb/s)/µs is at least 8.1x faster than the prior art.

05:15 PM

20-4
A 32Gb/s NRZ 37dB SerDes in 10nm CMOS to Support PCI Express Gen 5 Protocol

Mike Bichan[1]; Clifford Ting[1]; Bahram Zand[1]; Jing Wang[1]; Ruslana Shulyzki[1]; James Guthrie[1]; Katya Tyshchenko[1]; Junhong Zhao[1]; Alireza Parsafar[2]; Eric Liu[1]; Aynaz Vatankhahghadim[1]; Shaham Sharifian[1]; Aleksey Tyshchenko[1]; Michael De Vita[2]; Syed Rubab[1]; Sitaraman Iyer[2]; Fulvio Spagna[2]; Noam Dolev[3]
[1]Intel Toronto; [2]Intel Santa Clara; [3]Intel Chandler

The first SerDes design to demonstrate a PCI-Express 5 link with area of 0.33mm2 per lane, die edge usage per lane of 285 um, dynamic junction temperature range from -40C to 125C, energy efficiency of 11.4pJ/bit including PLL and clocking, power management including power gating for all analog blocks, continuous data rate support between 1-32 Gb/s, and supporting channel topologies with insertion loss up to 37dB at 16GHz with BER < 1e-12 in 10nm process.

Tuesday, March 24, 2020, 03:30 PM–05:30 PM

Session 21: Forum: Advances in 5G and Wireless Systems

Sponsored by SiFive
Session Chair: Xuanyao (Kelvin) Fong

4:00 PM-4:30 PM

21-1
Antenna-Electronics Co-Design — Multi-Feed Antennas Based Mm-Wave Front-Ends for On-Antenna Power Combining, Active Load Modulation, and Polarization Division Duplexing
Taiyun Chi, Dept. of Electrical & Computer Engineering, Rice University

4:00 PM-4:30 PM

21-2
Full-Duplex Radio Transceivers
Sudip Shekhar, Dept. of Electrical & Computer Engineering, University of British Columbia, BC, Canada

4:30 PM-5:00 PM

21-3
Resource Management in Wireless Networks via Multi-Agent Deep Reinforcement Learning
Dr Hosein Nikopour, Intel Labs

5:00 PM-5:30 PM

21-4
Creating a High-Frequency Design Platform to Meet Industry Wide Design Challenges
Michael Thompson, Cadence Design Systems

Wednesday, March 25

Wednesday, March 25, 2020, 09:40 AM–12:05 PM

Session 23: Oversampled Data Converters

Session Chair: Vanessa Chen, Carnegie Mellon University
Session Co-Chair: Ayman Shabra, MediaTek

This session includes papers on oversampled low-pass and bandpass converters with discrete-time and continuous-time processing. Techniques such as time-interleaving and pipelining are utilized in SAR based designs. In addition, a method that shapes pipeline inter-stage gain errors is presented.

09:30 AM

Introduction: Oversampled Data Converters

09:35 AM Best Invited Paper Candidate

23-1
Continuous-Time Bandpass Delta-Sigma Modulators and Bitstream Processing

Michael Flynn[1]; Rundao Lu[1]; John Bell[1]; Daniel Weyer[2]; Hyungil Chae[3]; Sunmin Jang[4]; Jaehun Jeong[5]

[1]University of Michigan; [2]Silicon Labs; [3]Kookmin University; [4]Apple; [5]Broadcom

Continuous-Time Bandpass Delta-Sigma Modulators (CTBPDSMs) are effective for IF sampling and simplify receiver design. Bitstream processing (BSP) can be combined with an array of CTBPDSMs to enable highly area and power efficient digital beamforming. BSP directly processes the raw bit-stream outputs of the quantizers, enabling digital processing with simple MUXs. The combination of BSP and CTBPDSMs is also effective in a digital PLL. Emerging techniques show the promise of multi-band noise-shaping in a CTDSM.

10:25 AM Best Student Paper Candidate

23-2
A 20 MHz Bandwidth Continuous-Time Delta-Sigma ADC Achieving 82.1 dB SNDR and >100 dB SFDR Using a Time-Interleaved Virtual-Ground-Switched FIR Feedback DAC

Alok Baluni[1]; Shanthi Pavan[1]

[1]Indian Institute of Technology, Madras

We present a single-bit continuous-time delta-sigma ADC that achieves 82.1dB peak SNDR and 101.2dB SFDR in a 65nm CMOS process. The key technique that enables low distortion is the use of a virtual-ground-switched resistive FIR feedback DAC, which operates in a 4x time-interleaved manner to reduce power dissipation. Interleaving artifacts, caused by mismatch, are addressed by mixed-signal calibration. The modulator and decimator consume 11.4mW and 15mW from 1.1V respectively. The Schreier FoM is 174.1dB.

10:50 AM

23-3
A 80dB DR 6MHz Bandwidth Pipelined Noise-Shaping SAR ADC with 1-2 MASH Structure

Sein Oh[1]; Younggyun Oh[1]; Juyong LEE[1]; Kihyun Lee[1]; Seungjun LEE[1]; Jintae Kim[2]; Hyungil Chae[2]
[1]Kookmin university; [2]Konkuk university

A pipelined NS-SAR ADC with 1-2 MASH structure is presented. Two-stage pipelined structure consisting of 5-bit NS-SAR and 4-bit NS-SAR ADCs shows 3rd-order noise-shaping. The measured DR is 80dB when the sampling rate is 83.3MS/s and bandwidth is 6MHz, and power consumption is 3.5mW showing FoM of 173.2dB. The proposed structure greatly relaxes design requirement of each SAR quantizer and helps to achieve high resolution as well as low power consumption and wide bandwidth.

11:15 AM Best Student Paper Candidate

23-4
A 77.1-dB 6.25-MHz-BW Pipeline SAR ADC with Enhanced Interstage Gain Error Shaping and Quantization Error Shaping

Chen-Kai Hsu[1]; Xiyuan Tang[1]; Wenda Zhao[1]; Rui Xu[1]; Abhishek Mukherjee[1]; Timothy Andeen[1]; Nan Sun[1]
[1]The University of Texas at Austin

This paper presents an enhanced interstage gain error shaping technique that adopts a digital error feedback technique to extend the interstage gain error tolerance by 5 times. This paper also proposes a passive quantization error shaping technique that reduces the ratio of a two-input-pair comparator by 2.7 times. A prototype equipped with the proposed techniques is implemented in 40nm CMOS achieving a SNDR of 77.1 dB over 6.25-MHz bandwidth and a 173.7 dB Schreier FoM.

11:40 AM

23-5
A Fully-Dynamic Time-Interleaved Noise-Shaping SAR ADC Based on CIFF Architecture

Haoyu Zhuang[1]; Jiaxin Liu[1]; Nan Sun[2]
[1]Tsinghua University; [2]University of Texas at Austin

This paper presents a fully-dynamic, low-power, and wide-band time-interleaved noise-shaping SAR ADC based on the cascade of integrators with feed-forward (CIFF) architecture. Its loop filter and interleaving operation are realized by fully-passive switched capacitor circuits. Its feedforward summation is implemented by using a multi-path comparator. Moreover, its overall NTF is set by device ratios and highly robust against PVT variations. It allows the loop filter poles to be placed close to the unit circle.

Wednesday, March 25, 2020, 09:30 AM–12:05 PM

Session 24: GaN and High-Voltage Power Converters

Session Chair: John Pigott, NXP Semiconductors

Session Co-Chair: Saurav Bandyopadhyay, Texas Instruments

This session has 5 papers presenting GaN converters and high voltage full ICs. The session starts with a 3 W 13x boost converter using a hybrid switching topology. Next is MEMS actuator supply generating up to 117 V from integrated PV cells in an SOI process. Paper 3 is a dual rail AMOLED power supply with 1 mV ripple. Following is a novel resonant dual inductor 48 W buck boost converter. Finishing the session is an invited paper presenting solutions to reliably drive GaN FETs through inductive parasitics in the gate loop.

09:30 AM

Introduction: GaN and High-Voltage Power Converters

09:35 AM

24-1
A 91% efficient 30V hybrid boost-SC converter based backlight LED driver in 180nm CMOS

Nilanjan Pal[1]; Adam Fish[2]; William McIntyre[2]; Nathanael Griesert[2]; Greg Winter[2]; Travis Eichhorn[2]; Robert Pilawa-Podgurski[3]; Pavan Hanumolu[1]

[1]University of Illinois at Urbana-Champaign; [2]Texas Instruments Incorporated; [3]University of California at Berkeley

This paper presents a 30V output hybrid boost converter-based LED driver for mobile displays using a synchronous inductive boost stage followed by a time-interleaved 1-2 series-parallel SC stages. This topology reduces switching losses by allowing the use of switches with low voltage-rating. Fabricated in a 180nm CMOS process, the prototype converter achieves 91.15% efficiency, which is 3% more than state-of-the-art.

10:00 AM

24-2
An 80-117V Pseudo-Adiabatic Drive Circuit for Microrobotic Actuators with Optical Power Delivery and Peak Power Reduction Factor over 14x

Yanqiao Li[1]; Jason Stauth[1]; Benjamin Dobbins[1]

[1]Dartmouth College

This work presents an efficient high-voltage drive circuit, a reconfigurable series-parallel switched-capacitor DC-DC converter, for mm-scale electrostatic and piezoelectric microrobotic transducers. The switched-capacitor converter boosts a nominal 5-7.4V input by ~16x to 80V-117V. By charging the output sequentially and recovering charge in discharge cycles, the converter reduces power consumption by over 14x compared to a conventional hard-switching driver. Measured results show effective operation with loads up to 20nF and operating frequency over 50kHz.

10:25 AM

24-3
A Power-Efficient Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays

Fangyu Mao[1]; Yan Lu[1]; Edoardo Bonizzoni[2]; Filippo Boera[2]; Mo Huang[1]; Franco Maloberti[2]; Rui Martins[1]

[1]University of Macau; [2]University of Pavia

This paper presents a hybrid SIBO DC-DC converter for AMOLED displays which are relatively more sensitive to their positive supply noises. This design significantly improves the display quality by achieving a near-zero ripple at the positive output thanks to the negative output floating and the low-power shunt regulators. With the hybrid topology and the proposed cross-coupled bootstrap-based level-shifter with a dual-PMOS inverter buffer, low-voltage devices without deep-N-well are used, reducing the chip area and cost.

10:50 AM Best Student Paper Candidate

24-4
A 9 - 45V Input 2MHz 3-Switch ZVS Step-up/down Hybrid Converter with 5x Volume Reduction

Chen Chen[1]; Jin Liu[1]; Hoi Lee[1]

[1]The University of Texas at Dallas

A new 3-switch ZVS step-up /-down hybrid converter is proposed to use 1 auxiliary branch to establish ZVS and reduce the conduction loss in the step-down mode. The proposed converter is verified to achieve peak power efficiencies of 98% and 96% at 2MHz in step-down and –up modes, respectively, over an input range of 9V – 45V. The volume of external components in the converter is reduced by 5 times compared with the prior art.

11:15 AM Invited Paper

24-5
Long, Short, Monolithic - The Gate Loop Challenge for GaN Drivers

Maik Kaufmann[1]; Achim Seidel[1]; Bernhard Wicht[1]

[1]Leibniz University Hannover

With fast-switching GaN any parasitic gate-loop inductance degrades the switching performance and may lead to false turn-on as well as gate-voltage overshoot. Two approaches to overcome these challenges in driving GaN transistors are discussed. In a discrete silicon-based driver, the gate-loop inductance is actively utilized for a resonant gate-drive approach. In a second implementation, the gate-loop inductance is reduced close to zero by GaN-on-Si monolithic integration of the power transistor and the driver on one die.

Wednesday, March 25, 2020, 09:30 AM–11:40 AM

Session 25: Analog in Advanced Technologies

Session Chair: Stefano Pietri, NXP Semiconductors

Session Co-Chair: Mark Oude Alink, University of Twente

The papers in this session describe design techniques for analog IC building blocks in 28nm or lower process nodes. They include two invited papers on ESD design challenges and papers on a voltage reference, a temperature sensor, and a low power PLL.

09:30 AM

Introduction: Analog in Advanced Technologies

09:35 AM Invited Paper

25-1
Technology Scaling of ESD Devices in State of the Art FinFET Technologies

Sukjin Kim[1]; Radhakrishnan Sithanandam[1]; Woojin Seo[1]; Mijin Lee[1]; Sangyoung Cho[1]; Juho Park[1]; Hyukhoon Kwon[1]; Namho Kim[1]; Chanhee Jeon[1]

[1]Samsung Foundry

Continuous optimization of power, performance and area lead to the evolution of planar CMOS to the FinFET technology. This paper presents challenges and solutions for robust ESD protection in FinFET technology. ESD devices of the general purpose I/O's and failsafe I/O's are analyzed in 14nm, 10nm and 7nm FinFET technologies, and a new charge-based CDM analysis strategy which ensures first time silicon success is also explained.

10:00 AM Invited Paper

25-2
ESD Protection Design Overview in Advanced SOI and Bulk FinFET Technologies

You Li[1]; Meng Miao[1]; Robert Gauthier[1]

[1]Globalfoundries

The FinFET era brings new challenges to ESD protection. An overview of ESD design in advanced SOI and bulk FinFET technologies is presented. The design innovations and device optimizations are explored to achieve an effective ESD protection. The predictive ESD modeling and simulations are studied to optimize ESD protection and ensure first-time-right chip ESD design in FinFET technologies.

10:25 AM

25-3
A 6-Transistor Ultra-Low Power CMOS Voltage Reference with 0.02 %/V Line Sensitivity

Hayden Bialek[1]; Matthew Johnston[1]; Arun Natarajan[1]

[1]Oregon State University

This work presents a technique for the design of ultra-low power CMOS voltage references achieving low line sensitivity while maintaining state-of-the-art temperature insensitivity. The 6-T voltage reference occupies only 840µm2 and consumes 28.6pA from a 0.5V supply. Measurements show an average line sensitivity of 0.02 %/V and an average temperature coefficient of 99.2 ppm/°C.

10:50 AM

25-4
A 0.5V-to-0.9V 0.2GHz-to-5GHz Ultra-Low-Power Digitally-Assisted Analog Ring PLL with Less Than 200ns Lock Time in 22nm FinFET CMOS Technology

Bo Xiang[1]; Yongping Fan[1]; James Ayers[1]; James Shen[1]; Dan Zhang[1]
[1]Intel Corporation

This paper presents an ultra-low power digitally-assisted analog ring phase-locked loop for microprocessors with a tunable switched capacitor loop filter. It achieves a power efficiency of 0.213mW/GHz and FoM of -234.4 dB with only 200ns lock time using a 100MHz reference clock. It supports a wide reference clock frequency range from 20MHz to 200MHz and can operate on a single 0.5-0.9V supply.

11:15 AM

25-5
A DTMOST-based Temperature Sensor with 3-sigma Inaccuracy of ±0.9℃ for Self-Refresh Control in 28nm Mobile DRAM

Sungsik Park[2]; Sungsik Park[1]; Yunhong Kim[1]; Yunhong Kim[2]; Woojun Choi[1]; Yongtae Lee[1]; Sungbeen Kim[2]; Youngmin Shin[2]; Youngcheol Chae[1]
[2]Samsung Electronics; [1]Yonsei University

This paper presents a compact temperature sensor that directly controls a temperature-dependent self-refresh period of a mobile DRAM in 28nm CMOS.It uses a supply independent relaxation oscillator based on capacitive discharge through a diode connected MOS transistor. The sensor occupies 0.017mm2 and achieves an accuracy of ±0.9°C from -10 to 90°C after 1-point trim. It operates from 0.85 to 1.15V supply, it has a supply sensitivity of 0.27°C/V at room temperature and it consumes 33.75µW.

Wednesday, March 25, 2020, 09:30 AM–11:40 AM

Session 26: Technology Oriented Design Foundations

Session Chair: Farhana Sheikh, Intel Circuit Research Lab
Session Co-Chair: Jaydeep P Kulkarni, The University of Texas at Austin

New technologies, models and circuits are presented to enable future applications in mmWave, THz, Quantum Computing, Security and Machine Learning.

09:30 AM

Introduction: Technology Oriented Design Foundations

09:35 AM

26-1
A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm for High Throughput Applications

Nael Mizanur Rahman[1]; Edward Lee[1]; Venkata Chaitanya Krishna Chekuri[1]; Arvind Singh[1]; Saibal Mukhopadhyay[1]

[1]*Georgia Institute of Technology*

A dual-mode PRINCE encryption cipher is implemented, in 65nm technology, that is configurable between pipelined and fully unrolled modes. Correlation Power and EM analysis on test-chip measurements show minimal exploitability of leakage from intermediate registers in pipelined mode. The pipelined designs exhibit similar side channel resistance to unrolled designs while providing higher frequency and throughput. The overall system has a minimum MTD of 460K and a projected maximum throughput of 492 Mega encryptions per second

10:00 AM

26-2
Design-Space Exploration of Quantum Approximate Optimization Algorithm under Noise

Mahabubul Alam[1]; Abdullah Ash-Saki[1]; Swaroop Ghosh[1]

[1]*Pennsylvania State University*

Quantum approximate optimization algorithm (QAOA) is a promising quantum-classical hybrid technique in near-term gate-based noisy quantum devices. In QAOA, the gate parameters of a parameterized quantum circuit are varied by a classical optimizer to generate a quantum state with significant support to the optimal solution. The existing analysis fails to consider non-idealities in the qubit quality. In this article, we study the impact of various noise sources on the performance of QAOA.

10:25 AM Invited Paper

26-3
Intel 22nm Low-Power FinFET (22FFL) Process Technology for 5G and Beyond

Hyung-Jin Lee[1]; Steven Callender[1]; Said Rami[1]; Woorim Shin[1]; Qiang Yu[1]; Jose Mauricio Marulanda[1]

[1]*Intel Corporation*

The paper introduces Intel's 2nd generation 22nm low-power FinFET technology (22FFL) developed for RF and mmWave applications. Intel's 22FFL is the comprehensive FinFET technology offering the best-in-class RF transistors reaching above 300GHz and 450GHz of ft and fmax respectively. The addition of the high-power RF device (HyPowerFF) and elaborated mmWave BEOL support the opportunity to push silicon technology beyond 5G era.

11:15 AM

26-4
A 16K Current-Based 8T SRAM Compute-In-Memory Macro with Decoupled Read/Write and 1-5bit Column ADC

Chengshuo Yu[1]; Chengshuo Yu[2]; Taegeun Yoo[1]; Tony Tae-Hyoung Kim[1]; Kevin Chai[2]; Bongjin Kim[1]

[1]*Nanyang Technological University;* [2]*Institute of Microelectronics (IME), A*STAR*

A novel 8T SRAM bitcell is proposed for computing dot-products based on current-mode accumulation. The read and write disturb issue has been eliminated by adding two extra transistors into a standard 6T SRAM bitcell. Besides, ADC overhead issue has been addressed using a column ADC embedded in

each column-based neuron. The column ADC output resolution is reconfigurable from 1-to-5bit. A test-chip is fabricated using 65nm, and the energy-efficiency of bitwise operation is 490-to-15.8TOPS/W at 1-5bit.

Wednesday, March 25, 2020, 12:05 PM–02:00 PM

Lunch Break

Wednesday, March 25, 2020, 02:00 PM–02:15 PM

Closing and Awards Ceremony

General Information

Registration
Registration entitles the registrant entrance to all Sunday Educational Sessions and the Monday – Wednesday Technical Sessions, Monday Welcome Reception, Tuesday Conference Reception, and a link to the digital proceedings.

Questions on Your Registration
If you have questions on your registration please contact:
By email: j.teehan@ieee.org
By phone: 732-465-6496

Onsite Registration is required for virtual admittance to all sessions.

Sunday, March 22	7:30 am - 5:00 pm
Monday, March 23	8:00 am - 5:00 pm
Tuesday, March 24	8:00 am - 5:00 pm
Wednesday, March 25	8:00 am - 11:00 am

CICC Keynote Luncheon
Monday, March 23 12:10 pm-2:00 pm

Lawrence E Larson, *Sorensen Family Dean of the School of Engineering, Brown University*
Title: Microelectronics for Brain-Computer Interface Applications

Abstract: As integrated circuit technology becomes increasingly deployed to address the challenges of human health, the opportunity to interface directly to the brain is one of the most exciting and high impact opportunities. Challenges like epilepsy, paraplegia, quadriplegia, locked-in syndrome, MLS, Parkinsons, and many others, are being addressed by this new technology. The recent announcement of significant advances by Neuralink is one example of the potential.This talk will summarize some of the challenges and opportunities of brain-computer-interface (BCI) technology from an integrated circuit perspective.

Bio: Larry Larson received his B.S. from Cornell University and his Ph.D. from UCLA. From 1980 to 1996, he was with Hughes Research Laboratories, Malibu, CA, USA, where he directed the development of high-frequency microelectronics in GaAs, InP, Si/SiGe, and MEMS technologies. In 1996, he joined the faculty of the University of California at San Diego (UCSD), where he was the inaugural holder of the Communications Industry Chair. From 2001 to 2006, he was Director of the UCSD Center for Wireless Communications, and from 2007 to 2011, was Chair of the Department of Electrical and Computer Engineering. In 2011, he joined Brown University, Providence, RI, USA, where he is Sorensen Family Dean of the School of Engineering. He has authored or coauthored over 300 papers and has coauthored four books. He holds over 40 U.S. patents.

For Further Information Contact

John Teehan, CMP, IEEE MCE	or	Danielle Corrigan, IEEE MCE
Tel: 732-465-6496		Tel: 732-562-6047
Email: j.teehan@ieee.org		Email: d.corrigan@ieee.org