Sunday, April 14

Educational Sessions

Educational Session 1 - Power Management Fundamentals

Salon D
Organizer: Dina El-Damak, University of Southern California
Co-Organizer: Tufan Karalar, Istanbul TU

ES1-1
8:30 – 10:00 am
High Voltage Devices, Topologies, and Gate Drivers, Yogesh Ramadass, Texas Instruments
Power electronics can be found in everything from electric vehicles and industrial motors, to laptop power adaptors that hook up to the wall outlets. While silicon still dominates the power semiconductor landscape, the recent onset of wide bandgap semiconductor (WBG) devices promises low loss, higher frequency operation of converters leading to smaller, lighter power supplies. This tutorial will introduce the properties of high voltage (200-1200V) Si superjunction and WBG devices and discuss their relative merits. The common power converter topologies employed in power systems will be explored with a detailed analysis of the main loss mechanisms inside a converter and the impact of topology and device choice on efficiency and power density. The latter part of the tutorial will discuss gate drive and associated protection circuits that are required to safely operate the power FETs with examples provided from commercial gate driver designs

ES1-2
10:30 – 12:00 pm
Wireless Power Transfer: Analysis and IC Design, Wing-Hung Ki, HKUST
Wireless power transfer (WPT) can be deployed for micro-watt applications such as RFID, and for kilo-watt applications such as electric vehicle (EV) wireless charging. In this talk, design-oriented analysis and modeling of coupled-coils will be discussed. For milli-watt applications such as implantable medical devices (IMDs), related IC techniques in designing active rectifiers and reconfigurable rectifiers will be presented, and local and global power control methods will be introduced. Wireless charging of mobile phone requires an output power of 5W, and as high as 15W for fast charging. Topological study in integrating the rectification stage with the voltage regulation stage will be presented, and related IC techniques will be discussed.

ES1-3
1:00 – 2:30 pm
Power Management for Low Power Sensors, Patrick Mercier, University of California, San Diego
Small, ultra-low-power integrated circuits afford new opportunities to sense and interact with the environment in new and exciting ways – for example by sensing quantities like temperature, humidity, or chemical concentrations in the environment or on the human body, by connecting instruments via short- or long-range wireless standards, by probing brain matter across arbitrary 3D geometries, and beyond. In all such applications, small and efficient power management solutions are required. In this presentation, we will discuss design techniques and example implementations of switched-capacitor, single-inductor multi-output (SIMO), and hybrid multi-level DC-DC converters that can achieve high efficiency in small sizes. Techniques to achieve high efficiency across wide dynamic power ranges will also be covered. Finally, we will discuss emerging trends on energy harvesting transducers and efficient multi-modal energy harvesting circuit solutions.

ES1-4
3:00 pm – 4:30 pm
Portable and Scalable High Voltage Circuits for Automotive Applications in BiCMOS Processes, Sri Navaneeth Easwaran, Texas Instruments
The electronic content is increasing in automotive applications replacing earlier mechanical and hydraulics solutions. However proper protection and diagnostic circuits are required to ensure that electronic components perform the expected function and achieve ultimate fail silent operation. Topology wise, these automotive circuits are not much different from the conventional analog circuits used in consumer electronics, but have to handle a

wide range input voltage from 5V to 40V and wide range of currents from 30mA to 4A. There are several additional system requirements and design implementation challenges that have to be considered when defining and implementing automotive safety circuits. This tutorial introduces the State of the Art requirements of automotive ICs.

The design of the ICs introduces the power stages and their driver along with challenges due to R-L-C type of loads with the design solutions is presented. Such designs need a good understanding of the junction temperature rise during the operation of power stages, and therefore an insight to thermal simulations will be presented. Test cases from high side driver, low side driver, configurable high side/low side floating drivers will be presented. These are used in several automotive applications for airbag, braking, power steering and solenoid drivers.

After discussing the power stages, the biasing circuitry for these power stages is covered. The power supply sequencing and various fault scenarios will be presented. A robust solution using the current and voltage selector based circuits will be discussed. Following the biasing circuits overview, the tutorial takes a deep look into the high voltage and negative voltage tolerant switches that are implemented for diagnostics in automotive applications. The tutorial covers design methodologies for implementing robust and safe switches that cannot be turned on or turned off inadvertently. Finally the tutorial presents programmable and scalable nature of these designs.

Structures for the proof of concept are simulated and measured. Tutorial does cover the strong and thermally activated parasitic bipolar transistor that gets activated unintentionally due to the negative voltage requirements. The aggressor and victim concepts will be presented from test cases. Such unintentional activation can cause catastrophic fails to the system and the tutorial presents the design and layout based mitigation methodology to avoid the interference of these parasitic in any technology node. This tutorial will be valuable for the design community in general to carefully design high voltage fault tolerant circuits not only limited to automotive but also for industrial and personal electronics.

Educational Session 2 - What You Need to Know to Design Effectively in 10 nm and Beyond

Room 408
Organizer: Jiangfeng Wu, Tongji University Shanghai China
Co-Organizer: Colin McAndrew, NXP Semiconductors

ES2-1
8:30 – 10:00 am
IC Design after Moore's Law, Greg Yeric, ARM

ES2-2
10:30 – 12:00 pm
Nanoscale CMOS Implications on Analog/Mixed-Signal Design, Alvin Loke, Qualcomm

ES2-3
1:00 – 2:30 pm
Developing Analog Circuit Generators using the Berkeley Analog Generator Framework, Eric Chang, UC Berkeley

ES2-4
3:00 pm – 4:30 pm
ESD in FinFET and Gate-All-Around Transistors, going from 14nm to 3nm, Shih-Hung Chen, IMEC

Educational Session 3 - 56/112G Link Foundations

Room 410
Organizer: Sudip Shekhar, University of British Columbia

Co-Organizer: Shreyas Sen, Purdue University

ES3-1
8:30 – 10:00 am
Standards, Link Budgeting and Modeling, Ganesh Balamurugan, Intel

ES3-2
10:30 – 12:00 pm
Optical Links, Azita Emami, California Institute of Technology

ES3-3
1:00 – 2:30 pm
ADC-based Wireline Transceivers, Yohan Frans, Xilinx

ES3-4
3:00 pm – 4:30 pm
Mixed-signal electrical interfaces, Elad Alon, University of California Berkeley

Educational Session 4 - Machine Learning, Quantum,and Security Hardware

Salon E
Organizer: Rajiv Joshi, IBM
Co-Organizer: Gregory Chen, Intel

ES4-1
8:30 – 10:00 am
New Frontiers in Hardware Security in the IoT Regime, Swarup Bhunia, University of Florida
Security has become a critical design challenge for modern electronic hardware. With the emergence of the Internet of Things (IoT) regime that promises exciting new applications from smart cities to connected autonomous vehicles, security has come to the forefront of the system design process. Recent discoveries and reports on numerous security attacks on microchips and circuits violate the well-regarded concept of hardware trust anchors. It has prompted system designers to develop wide array of design-for-security and test/validation solutions to achieve high security assurance for electronic hardware. At the same time, emerging security issues and countermeasures have also led to interesting interplay between security, verification, and interoperability. Verification of hardware for security and trust at different levels of abstraction is rapidly becoming an integral part of the system design flow. The global economic trend that promotes outsourcing of design and fabrication process to untrusted facilities coupled with the prevalent practice of system on chip design using untrusted 3rd party IPs, has given rise to the critical need of trust verification of IPs, system-on-chip design, and fabricated chips. The talk will also cover the spectrum of security challenges for IoTs and describe emerging solutions in creating secure trustworthy hardware that can enable IoT security for the masses.

ES4-2
10:30 – 12:00 pm
Mobile Deep Learning Processors on the Edge, Hoi-Jun Yoo, KAIST
Recently, Deep Learning is changing not only the technology paradigm in electronics but also the society itself with Artificial Intelligence technologies.

In this lecture, firstly, the status of AI and DNN SoCs will be reviewed from two perspectives; the data-center oriented and the mobile and embedded AIs. This dichotomy shows clearly the possible application areas for the emerging future AIs. Especially, mobile and embedded deep learning hardware, CNPU, DNPU and UNPU will be introduced together with CNN (Convolutional Neural Network) and RNN (Recurrent Neural Network). In addition, their high efficiency and flexibility with “Dynamically Reconfigurable Processor” architecture will be explained in detail with the real chip measurement results.

Secondly, KAIST's approach integrating both sides of brain, right-brain for "approximation and adaptation hardware" and left-brain for "precise and programmable Von Neumann architecture", will be explained with novel design methodology. The deep neural networks and the specialized intelligent hardware (mimicking right brain) capable of statistical processing or learning and the multi-core processors (mimicking left brain) performing the precise computations including software AI are integrated on the same SoC.

ES4-3
1:00 – 2:30 pm
Introduction to Compute-in-Memory, Dave Fick and Laura Fick, Mythic-AI
AI and many other applications have opportunities to build systems that merge memory and computing into a unified structure in ways which yields significant improvements in energy efficiency, performance, and cost. In these scenarios, "moving the compute to the memory" makes sense because the applications have large amounts of data to process and relatively simple operations to perform, which makes it not too difficult to create specialized processing near the memory when traditionally moving the data to the main system processor would be slow and inefficient. These scenarios have a have a wide variety of applications as well as approaches. On one end of the spectrum, systems which have processing inside of an SSD to perform searches inside the drive itself, and on the other end of the spectrum, systems that have analog compute performing mathematics directly on the bitlines of the memory arrays. In this talk we will provide an overview of many of these approaches as well as the methods to their madness.

ES4-4
3:00 pm – 4:30 pm
Quantum Technology Overview, Mark Ritter, IBM
There are three rubrics of quantum technology: quantum communication, quantum sensing, and quantum computation. I will present an overview of these three areas, then focus on technologies for quantum computation. I will briefly describe the properties of qubits that promise a leap in computational power for certain problems. Then I will review the details and current status of a number of qubit technologies, including how they are controlled and measured by microwave or optical signals. I will describe single and two-qubit gates—all that is necessary to create universal quantum logic circuits—and basic algorithms which exploit superposition and entanglement of quantum information. I will then take a system-level view, describing the challenges of controlling and measuring systems of qubits. Finally, we will look at the basic types of universal quantum computers: near-term Noisy Intermediate Quantum systems (NISQ), and fully error-corrected Fault Tolerant Quantum Computers (FTQC), the types of algorithms that can be run on these machines and the estimated system resource to run different algorithms.

Monday, April 15

Session 1 – Plenary Session

Monday, April 15, 8:00 am, Salon D/E
General Chair: Alessandro Piovaccari
Conference Chair: Hua Wang, Georgia Insitute of Technology
Program Chair: Fa Foster Dai, Auburn University

8:00 am
Welcome and Opening Remarks: Alessandro Piovaccari, Silicon Labs, General Chair and Hua Wang, Georgia Institute of Technology, Conference Chair
Award Presentations
Keynote Speaker Introductions: Alessandro Piovaccari, Silicon Labs, General Chair

8:20 am
Keynote Speaker: The DARPA Electronics Resurgence Initiative, Dr. Stephen Trimberger, DARPA Program Manager

The microelectronics community is facing an array of long-foreseen obstacles to the transistor scaling that has allowed for 50 years of rapid progress in electronics. Current economic, geopolitical, and physics-based complications make the future of the electronics industry uniquely interesting at this moment. To jump-start innovation in the field, DARPA announced in June 2017 that it would coalesce a broad series of programs into the Electronics Resurgence Initiative (ERI). ERI calls for innovative new approaches to microsystems materials, designs, and architectures. Underscoring the importance of the initiative, the President's budget for FY19 includes continued annual investments of $300 million over five years for ERI's research efforts–potentially upwards of $1.5 billion over the initiative's lifetime. The first round of programs is underway at a number of corporate and university research institutions. This presentation describes the background, rationale and major focus areas of ERI, with discussion of activities in the first round of programs.

9:10 am
Keynote Speaker: What Machine Learning needs from Embedded Hardware, Pete Warden, Tech Lead, Mobile and Embedded TensorFlow

This talk will cover the unique demands that deep learning makes on microcontroller hardware. Machine learning workloads are very different from traditional computation, including very heavy arithmetic intensity with low memory usage, relaxed requirements on precision, lack of branching, and knowledge of memory access patterns for many millions of cycles ahead of time.

10:00 am BREAK

Session 2 - Millimeter-Wave and Sub-Terahertz Transceivers

Monday, April 15, 10:30 am, Salon D
Session Chair: Yahya Tousi, University of Minnesota
Session Co-Chair: Hossein Lavasani, Qualcomm

This session covers novel techniques for developing mm-wave and sub-THZ integrated transmitter and receivers with applications in high-speed wireless communication, radar, and sensing.

10:30 am
Introduction

10:35 am
2-1
Millimeter-Wave Transceivers for Wireless Communication, Radar, and Sensing (Invited), Aritra Banerjee[1], Kristof Vaesen[2], Akshay Visweswaran[2], Khaled Khalaf[2], Qixian Shi[2], Steven Brebels[2], Davide Guermandi[2], Cheng-Hsueh Tsai[2,3], Johan Nguyen[2,3], Alaa Medra[2,3,4], Yao Liu[2], Giovanni Mangraviti[2], Orges Furxhi[1], Bert Gyselinckx[1], Andre Bourdoux[2], Jan Craninckx[2], Piet Wambacq[2,3], [1]imec USA Nanoelectronics Design Center, [2]imec, Leuven, [3]Vrije Universiteit Brussel, [4]Qualcomm

Due to growing demand for higher data rates in wireless communication, high resolution requirement in radars, and emerging sensing applications, mm-wave frequency bands have become very attractive in recent years. Architectures and circuits of mm-wave transceivers are described and comparison of process technologies for mm-wave IC design is presented. Critical mm-wave circuit blocks and example implementations such as 60 GHz phased array, 28 GHz front-end, 79 GHz PMCW radar and 145 GHz FMCW radar are discussed and future trends are identified.

11:25 am
2-2

A Multi-Port Dual Polarized Antenna Coupled mm-Wave CMOS Receiver with Element-level Pattern and Notch Programmability and Passive Interferer Rejection Capability, X. Lu, X. Wu, H. Saeidi, K. Sengupta, Princeton University

Millimeter-wave based wireless communication and sensing systems for future 5G applications are expected to operate in a complex electromagnetic environment with dynamically changing near-field conditions. This is particularly true for user equipment where presence of near-field blockages and scatterers can significantly affect the front-end antenna and therefore the system performance. Classical beamforming architectures that rely on identical patterns on all elements can be extremely energy inefficient in such cases. Element-level pattern shaping that can dynamically reconfigure the properties of a single antenna can not only allow mitigation of such complex electromagnetic environment, but incorporate system properties that are distinct from classical arrays. In this work, we present a multi-port on-chip dual polarized antenna and a multi-port receiver co-design approach that allows dynamic pattern reconfiguration and element notch control that can reject interferers directly at the antenna surface before beamforming. We demonstrate this in state of the art receiver performance in a 65-nm CMOS process at 70 GHz with element maxima and notch tuning capability of more than 90 degree while allowing high sensitivity and minimizing impedance mismatches and power losses.

11:50 am
2-3
A 100-120GHz 20Gbps Bits-to-RF 16QAM Transmitter Using 1-bit Digital-to-Analog Interface, H. Wang, H. Mohammadnezhad, D. Dimlioglu, P. Heydari, University of California, Irvine.

A mm-wave wireless transmitter that takes raw data bits as input and generate 16QAM constellation by combining two QPSK constellations with an amplitude ratio of 2 is presented. The transmitter delivers 3dBm maximum CW output power. Wireless test at a distance of 20cm measures 20Gbps with an EVM of-15.8dB.

Session 3 - Oscillators and PLLs

Monday, April 15, 10:30 am, Salon E
Session Chair: Nagendra Krishnapura, IIT Madras
Session Co-Chair: Mark Oude Alink, University of Twente

This session features papers with low-temperature-coefficient oscillators and a fractional-n PLL with space-time averaging for quantification noise reduction.

10:30 am
Introduction

10:35 am
3-1
A 0.84pJ/cycle Wheatstone Bridge Based CMOS RC Oscillator with Reconfigurable Frequencies *(Outstanding Sutdent Paper Nominee)*, P. Chen, D. Li, Z. Yu, Q. Jin*, K. Yang, Rice University, *Xi'an Jiaotong University

A low-power CMOS RC relaxation oscillator supporting configurable frequencies is presented for timekeeping in low-power IoT applications. By employing a Wheatstone Bridge scheme, the design achieves an average temperature coefficient down to 9.6ppm/ºC at nominal 67kHz across -20ºC to 100ºC, and an energy efficiency of 0.84pJ/cycle.

11:00 am
3-2
A 107 µW MedRadio Injection-Locked Clock Multiplier with a CTAT-biased 126 ppm/°C Ring Oscillator, Somok Mondal and Drew A. Hall, University of California, San Diego

This paper presents a 400 MHz open-loop injection-locked clock multiplier (ILCM) with low-power and fast settling time. A one-time DCO calibration and novel temperature compensation scheme guarantees PVT-robustness without the use of a power-hungry conventional frequency tracking loop (FTL). The compensated ring oscillator exhibits a frequency stability of 126 ppm/°C over a 0 to 55 °C temperature range. This suffices to maintain lock and meet MedRadio specifications as indicated from measurements taken from 20 test chips. The chip was fabricated in 180 nm CMOS and

consumes 107 µW from a 0.7 V supply achieving state-of-the-art performance for PVT robust ILCMs operating at a comparable frequency range.

11:25 am
3-3
A 2.4-GHz ΔΣ Fractional-N Synthesizer with Space-Time Averaging for Noise Reduction, Yanlong Zhang[1,2,3], Arindam Sanyal[4], Xing Quan[3], Kailin Wen[3], Xiyuan Tang[2], Gang Jin[3], Li Geng[1], Nan Sun[2], [1]Xi'an Jiaotong University, [2]University of Texas at Austin, [3]Xidian University, [4]State University of New York at Buffalo,

This paper presents a novel highly digital technique to reduce the quantization noise of fractional-N PLLs at all frequencies. A frequency synthesizer with low power is implemented based on this technique. Measurement results clearly prove the effectiveness of this technique and show the synthesizer has a good performance.

11:50 am
3-4
A 68/36ppm/°C TC 32.768kHz-to-1MHz RC-based Oscillator with 72/6pJ Start-up Energy, H. Gomez, J.Arenas, C. Rojas, D. Reyes, A. Mantilla, E. Roa, Universidad Industrial de Santander

This paper describes a 32.768kHz-to-1MHz RC based oscillator (RCO) for high- and low-duty-cycle sleep-mode timers in emerging sensor node applications. Measurement shows a temperature stability of 68.5ppm/°C @32.768kHz and 37.5ppm/°C @1MHz, and an energy efficiency of 1.46nW/kHz@1MHz, occupying an area of 0.055mm2 in a pure digital 180nm CMOS process node.

Session 4 - Advanced Accelerators and Digital Design Techniques

Monday, April 15, 10:30 am, Room 408
Session Chair: Rajiv Joshi, IBM
Session Co-Chair: Carlos Tokunaga, Intel Corporation

This session covers a wide array of advanced digital accelerators and design techniques. It includes accelerators for AI, encoding as well as adaptive circuits for novel process platforms.

10:30 am
Introduction

10:35 am
4-1
OPTIMO: A 65nm 270MHz 143.2mW Programmable Spatial-Array-Processor with a Hierarchical Multi-cast On-Chip Network for Solving Distributed Optimizations, M. Chang, L. Lin, J. Romberg, A. Raychowdhury, Georgia Institute of Technology

We present a 49-core fully-programmable spatial array processor for solving distributed optimizations with support for a large class of algorithms and applications. We note a peak performance of 270MHz and peak energy-efficiency of 0.279 TOPS/W.

11:00 am
4-2
A 2048-Neuron Spiking Neural Network Accelerator with Neuro-Inspired Pruning and Asynchronous Network on Chip in 40nm CMOS, Sung-Gun Cho, Edith Beigné*, Zhengya Zhang, University of Michigan, *CEA-LETI

A 40nm, 2.56mm^2, 2048-neuron GALS SNN chip is presented. We allow neurons to specialize to excitatory or inhibitory, and apply distance-based pruning to cut communication and memory. An asynchronous router limits the latency to 1.32ns per hop. The chip achieves 7.85GSOP/s at 0.7V, consuming 5.9pJ/SOP.

11:25 am
4-3

A 220-900mV 179Mcode/s 36pJ/code Canonical Huffman Encoder for DEFLATE Compression in 14nm CMOS, Sudhir Satpathy, Vikram Suresh, Raghavan Kumar, Vinodh Gopal, James Guilford, Kirk Yap, Mark Anders, Himanshu Kaul, Amit Agarwal, Steven Hsu, Ram Krishnamurthy, Sanu Mathew, Intel

A 179Mcode/s canonical Huffman encoder for accelerating data compression is fabricated in 14nm CMOS. Unified literal-length and distance symbol processing, concurrent 2-stage sorting and binary tree construction, opportunistic symbol skipping with optimal register-file tagging, and in-line length-limitation eliminate serial data dependency enabling 1150 cycle latency, 17× faster than prior work.

11:50 am
4-4
A 0.5 V 2.5 uW/MHz Microcontroller with Analog-Assisted Adaptive Body Bias PVT Compensation with 3.13 nW/kB SRAM Retention in 55 nm Deeply-Depleted Channel CMOS, Marc Pons*, Christoph Müller* **, David Ruffieux*, Jean-Luc Nagel*, Stéphane Emery*, Andreas Burg**, Shuuji Tanahashi***, Yoshitaka Tanaka***, Atsushi Takeuchi***, *CSEM SA, **EPFL, ***Mie Fujitsu Semiconductor Limited.

In this paper we exploit strong body factor of deeply-depleted channel CMOS at 0.5V to compensate frequency over PVT to ±6%, achieving 30x frequency and 20x leakage scaling in a 2.56uW/MHz RISC-Core with 3.13nW/kB 2.5uW/MHz SRAM. Frequency-leakage configurability is implemented by current-controlled adaptive body bias at a fixed supply voltage.

Session 5 - Forum-New Paradigm in Miniaturized Electronics-Wearables and Neural Interfaces

Monday, April 15, 10:30 am, Room 410
Session Chair: Hansraj Singh
Session Co-Chair: Jerald Yoo, National University of Singapore

10:30 am
Introduction

10:35 am
5-1
Unawearables: Addressing Sensor, Circuit, and Energy Harvesting Challenges in Next-Generation Wearable Devices, Patrick Mercier, University of California San Diego

11:00 am
5-2
Circuits for ultrasonic neural interfacing at the micron scale, Rikky Muller, University of California, Berkeley

11:25 am
5-3
Electro-Quasistatic Human Body Communication: From Physics to Broadband IC and Applications, Shreyas Sen, Purdue University

11:50 am
5-4
Go with your Gut: Ingestible Wireless Sensors for Monitoring the GI Tract, Amin Arabian, Stanford University

Session 6 - RF Transmitter and Building Blocks

Monday, April 15, 1:30 pm, Salon D
Session Chair: Debopriyo Chowdhury, Broadcom
Session Co-Chair: Aritra Banerjee, IMEC

This session presents advanced RF transmitters and power amplifiers. It starts with an ultra-low-power TRX for implantables and moves on to high efficiency and wideband techniques for GHz transmitters and PAs.

1:30 pm
Introduction

1:35 pm
6-1
A 1.2 V Single Supply Hybrid Current-/Voltage-Mode Three-Way Digital Doherty PA with Built-In Large-Signal Phase Compensation Achieving Less-Than 5° AM-PM *(Outstanding Sutdent Paper Nominee)*, Doohwan Jung, Jongseok Park, Sensen Li, Tzu-Yuan Huang, Huan Zhao*, Hua Wang, Georgia Institute of Technology, *Kangxi Communication Technologies (Shanghai) Co., Ltd

This paper presents a single supply (1.2V) hybrid current-/voltage-mode three-way digital Doherty PA with built-in large-signal phase compensation technique to improve the power amplifier (PA) efficiency at deep power back-off, substantially reduce AM-PM distortion, and further simply supply power management. The design leverages one current-mode digital PA as the main path and two voltage-mode digital PAs as the two auxiliary paths, combining by three-way transformer-based series Doherty output network. As a proof-of-concept, the three-way hybrid digital Doherty PA is implemented in 45 nm CMOS SOI process occupying 3 mm-by-2 mm. It achieves +22.4 dBm peak output power together with 38.5/32.1/18.7% drain efficiency (DE) for the peak/3.4/9.3 dB output power back-off (PBO) at 2.3 GHz. The proposed digital Doherty PA demonstrates 1.26×/1.46× PBO efficiency enhancement, compared to an ideal class-B implementation at 3.4/9.3 dB PBO. The maximum AM-PM distortion is 4.7° at 2.3 GHz without using AM-PM look-up table (LUT). The measured EVM of 64-QAM/40 MHz and 256-QAM/10 MHz are -32 dB and -32.1 dB with 24.7% and 23.2% average DE without AM-PM LUT.

2:00 pm
6-2
An 8.5-11 GHz CMOS Transmitter with >19 dBm $OP1_{dB}$ and 24 % Efficiency, J. Li, R. Shu, Q. J. Gu, UC Davis

This paper presents the first reported highly linear, power efficient, and wideband X-band transmitter (TX) with a fully integrated power amplifier (PA) in 65 nm bulk CMOS. The TX features baseband current-bleeding, headroom-efficient and low-noise current mirror, harmonic trapping on the up-conversion mixer, wideband PA inter-stage matching (IM), bulk-floating connection on the PA output stage, as well as efficient output matching network. Fabricated in 65 nm bulk CMOS, the TX achieves 1dB bandwidth from 8.5 GHz to 11 GHz, >19 dBm OP1dB with 24 % system efficiency, and - 134.9/-135 dBm/Hz out-of-band noise for the lower and upper sidebands. To the author's best knowledge, this work is the highest efficiency X-band, PA-included TX in CMOS at OP1dB.

2:25 pm
6-3
A Wideband SAW-Less Transmitter Operating in Closed-Loop with Embedded N-Path Filtering, A. Coccia, L. Fanori*, D. Manstretta, R. Castello, University of Pavia, * Advanced Circuit Pursuit

A transmitter with >100MHz signal bandwidth is proposed for mobile terminals below 6GHz. Passive mixers with shunt-feedback RF amplifiers operate in closed-loop, improving linearity without pre-distortion. At Pout of 3dBm efficiency is 3.7%, ACLR is -40dBc, CIM3 is -49dBc and close-in noise is -153.5dBc/Hz.

2:50 pm
6-4
A 7×7×2mm^3 8.6-µW 500-kb/s transmitter with robust injection-locking based frequency-to-amplitude conversion receiver targeting for implantable applications, B. Xiong, Y. Li, A.Y.V. Thean, C.H. Heng, National University of Singapore

We present an I2O-BCC TX/RX pair for ultra-low power miniaturized implanted application. Injection locking based frequency-to-amplitude conversion characteristic is exploited to achieve robust RX demodulation despite TX frequency fluctuation due to no off-chip reference. The packaged TX is 7x7x2mm^3 and consumes only 8.6µW at 500kb/s, while the RX consumes 591.5µW.

3:15 pm - BREAK

Session 7 – Sensors and Interface Circuits

Monday, April 15, 1:30 pm, Salon E
Session Chair: Ping Gui, Southern Methodist University
Session Co-Chair: Maysam Ghovanloo, Georgia Institute of Technology

This session starts with a talk on inertial measurement unit chip, following by two readout circuits, three temperature sensors, and an accelerometer array.

1:30 pm
Introduction

1:35 pm
7-1
A 0.025-mm^2 0.8-V 78.5dB-SNDR VCO-based Sensor Readout Circuit in a Hybrid PLL-ΔΣM Structure, Shaolan Li, Wenda Zhao, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan, Nan Sun, The University of Texas at Austin

This paper presents a capacitive-coupled VCO-based sensor readout featuring a hybrid PLL-ΔΣM structure. It leverages phase-locking and PFD array to concurrently perform quantization and DEM, much reducing hardware/power compared to existing VCO-based readouts' counting scheme. A low-cost in-cell DWA scheme is presented to enable highly linear tri-level DAC. Fabricated in 40nm CMOS, the prototype readout achieves 78dB SNDR in 10kHz BW, consuming 4.5uW and 0.025mm2 active area. With 172dB Schreier FoM, its efficiency advances state-of-the-art VCO-based readouts by 50x.

2:00 pm
7-2
A 640 pW 22 pJ/sample Gate Leakage-Based Digital CMOS Temperature Sensor with 0.25°C Resolution, D.S. Truesdell, B.H. Calhoun, University of Virginia

This work presents a 640 pW, 22 pJ/conversion temperature sensor with 0.25°C resolution and -2.7/1.8°C worst-case inaccuracy from -20°C to 100°C. Gate leakage currents are utilized to drive both the sensing and sampling elements, enabling compact and reliable operation that balances low power and low energy for flexible application use.

2:25 pm
7-3
High-Q Timing and Inertial Measurement Unit Chip (TIMU) with 3D Wafer-Level Packaging (Invited), Farrokh Ayazi, Haoran Wen, Yaesuk Jeong*, Pranav Gupta, Anosh Daruwalla, Chang-Shun Liu, Georgia Institute of Technology, *Panasonic Device Solutions Laboratory of MA

This paper presents a high dynamic range timing and inertial measurement unit chip (TIMU) fabricated in a 3D nano-gap DRIE process and wafer-level-packaged (WLP) using a hermetic TSV interposer. High-Q gyroscopic resonators are dynamically tuned to enable tri-axial Coriolis gyroscopes with unprecedented sensitivity levels. Advanced interface circuit architectures enable self-calibration, hence reducing drift substantially.

3:15 pm - BREAK

3:30 pm
7-4
A 9-bit Resistor-Based All-Digital Temperature Sensor with a SAR-Quantization Embedded Differential Low-Pass Filter in 65nm CMOS Consuming 57pJ with a 2.5 µm Conversion Time, A. Wang, C. Chen, C.-J. R. Shi, University of Washington

This paper presents a resistor-based area-compact temperature sensor for on-chip thermal detection. It has three novel features: (1) a differential low pass RC filter (DLPF) for thermal sensing reducing the area; (2) the SAR-quantization is embedded in the DLPF reusing the capacitor in the DLPF for capacitive-DAC, eliminating DAC reference, and utilizing the full input range of the ADC, and (3) an all-digital circuit architecture which can be easily migrated to different processes. The temperature sensor was fabricated in a 65nm CMOS technology and achieved 0.4 °C resolution at the room temperature. After 2-point calibration with the removal of the systematic error, the sensor achieves a 3σ inaccuracy of ±1.2 °C from -30 to 100 °C. It consumes 22.8 µW power from 0.9V supply. With a 2.5 µs conversion time, the sensor achieves 57 pJ/Conversion energy efficiency, which yields 9 pJ·K^2 resolution FoM.

3:55 pm
7-5
Spatial Temperature Sensor with Distributed MASH Modulators, Hon-Piu Lam, Wing-Hung Ki, The Hong Kong University of Science and Technology

Local temperature sensors with the 1st-order noise-shaping readouts are spatially distributed to each hot-spot site. It can operate independently for the low-resolution temperature sensing or combine with an adjacent local sensor to form 2nd-order noise-shaping readouts for the better resolution and throughput.

4:20 pm
7-6
A High Dynamic Range CMOS-MEMS Accelerometer Array with Drift Compensation and Fine-Grain Offset Compensation *(Outstanding Regular Paper Nominee)*, Xiaoliang Li, Vincent P.J.Chung, Metin G. Guney, Tamal Mukherjee, Gary K. Fedder, Jeyanandh Paramesh, Carnegie Mellon University

This paper presents a high dynamic range CMOS-MEMS capacitive accelerometer. An array of small masses enables the accelerometer to survive and measure high-G (kG) acceleration. A fine-grain offset compensation technique suppresses the offset due to sense capacitance mismatch. The key idea is to employ two out of 184 accelerometer cells to tune out the charge imbalance, which ensures 90X improved tuning resolution (sub-aF offset). Multiple temperature sensors are integrated on the same accelerometer chip to improve the accelerometer long-term bias instability.

4:55 pm
7-7
A 14nV/√Hz 14µW Chopper Instrumentation Amplifier with Dynamic Offset Zeroing (DOZ) Technique for Ripple Reduction, Liang Fang, Ping Gui, Southern Methodist University

This paper presents a 14nV/√Hz instrumentation amplifier For Electroretinography application implemented in 180nm CMOS. A dynamic offset zeroing technique is proposed to suppress opamp input offset with negligible noise, power and circuit overhead. This design achieves a noise efficiency factor of 2.2 and consume 14µW power.

Session 8 - Wireline Clocking Techniques

Monday, April 15, 1:30 pm, Room 408
Session Chair: Mayank Raj, Xilinx
Session Co-Chair: Xiang Gao, Credo Semiconductor

This session showcases wireline clocking techniques such as IU generation, phase interpolation, clock multiplication and digital PLLs.

1:30 pm
Introduction

1:35 pm
8-1
A 5GHz 245fs$_{rms}$ 8mW Ring Oscillator-based Digital Frequency Synthesizer, A. Khashaba, A. Elkholy, K. M. Megawer, M. Ahmed, P. K. Hanumolu , University of Illinois at Urbana-Champaign

The phase noise of ring oscillator-based frequency synthesizers is limited by jitter accumulation. In this paper, we present a synthesizer architecture that uses a low noise passive multiphase generator and digital background calibration to synthesize a 245fsrms 5GHz output from a 54MHz crystal oscillator while consuming only 8.2 mW.

2:00 pm
8-2
A 2-to-20 GHz Multi-Phase Clock Generator with Phase Interpolators Using Injection-Locked Oscillation Buffers for High-Speed IOs in 16nm FinFET *(Outstanding Regular Paper Nominee)*, Sanquan Song*, John Poulton**, Xi Chen*, Brian Zimmer*, Stephen G. Tell**, Walker J. Turner**, Sudhir S. Kudva*, Nikola Nedovic*, John Wilson**, C. Thomas Gray**, and William J. Dally*, *NVIDIA Corporation, Santa Clara CA, **NVIDIA Corporation, Durham, NC

To support high-speed IOs, a 2-to-20 GHz cross-coupled inverter-based multi-phase PLL with phase interpolators using injection-locked oscillation buffers is presented. The proposed voltage-controlled oscillator (VCO) is made of two 4-stage ring oscillators (RO), where the introduction of feedback and cross-coupled resistances enable the VCO to run at higher speeds compared to a conventional 4-stage RO. Injection-locked oscillation buffering is proposed to restore swing and reduce duty cycle error (DCE) for VCO output buffers and PIs. Fabricated in 16nm process, it runs 25% faster and consumes 20% less power than prior works, with less than 1.8% DCE at 20 GHz across PI code range.

2:25 pm
8-3
A 14-GHz Bang-Bang Digital PLL with sub-150fs Integrated Jitter for Wireline Applications in 7nm FinFET, D. Pfaff, R. Abbott, X. Wang, B. Zamanlooy, S. Moazzeni, R. Smith**, C. Lin*, TSMC Ottawa Canada, *TSMC San Jose, **Carleton University

A digital look-ahead loop filter, operating at 3.5GHz, combined with a fine frequency resolution FinFET oscillator (1.2MHz/LSB) facilitates the low jitter performance of this 14GHz Bang-Bang PLL, only demonstrated previously in analog Charge Pump PLLs. Here, small area (0.06mm2) combined with 40mW dissipation complement the 143fs rms integrated jitter (1kHz-100MHz).

2:50 pm
8-4
A 5GHz 200kHz/5000ppm Spread-Spectrum Clock Generator with Calibration-Free Two-Point Modulation Using a Nested-Loop BBPLL, Xiaohua Huang, Kunnong Zeng, Yuguang Liu, Woogeun Rhee, Taeik Kim*, Zhihua Wang, Tsinghua University, *Samsung Electronics

This paper describes a 5GHz calibration-free two-point modulation method for SSCG by utilizing a two-stage nested-loop BBPLL architecture, featuring a 1-bit TDC and an absolute-gain DCO. Implemented in 65nm CMOS, the proposed SSCG achieves an EMI reduction of 26dB with 200kHz modulation frequency and 5000ppm frequency spread, consuming 9mW with 1V supply.

3:15 pm - BREAK

3:30 pm
8-5
Voltage-Follower Coupling Quadrature Oscillator with Embedded Phase-Interpolator in 16nm FinFET, X. Chen, S. Song, J. Poulton, N. Nedovic, B. Zimmer, S. Tell, C. Gray, NVIDIA Corporation

A phase-interpolator embedded quadrature oscillator was designed and tested. Voltage-follower based cross-coupling loops create tunable phase relationship among OSC-rings. The measurement results show that the PI-OSC provides 1.25/0.97 LSB INL/DNL performance at 24GHz while consuming only 8.1mW power. This compact oscillator is suitable for clock generation in high-speed low-power links.

3:55 pm
8-6

A 1.5pJ/bit, 5-to-10Gbps Forwarded-Clock I/O with Per-Lane Clock De-Skew in a Low Power 28nm CMOS Process, A. Jose, V. Abramzon, M. Elzeftawi, M. Wang, K. Kim, Y. Song, S. Moballegh, J. Kamali, A. Amirkhany, Samsung Semiconductor Inc.

This paper presents a 5-10Gbps forwarded-clock interface with per-lane clock de-skew utilizing a novel IQ-generation (IQ-gen) circuit as the RX front-end of the forwarded-clock path. The IQ-gen, used to restore a 250mV-pp TX clock over a 14dB-loss channel, generates I/Q clocks suitable for phase-interpolation with <1% IQ phase-error and 50mVpp sensitivity. The prototype TX and RX, fabricated in a 28nm LP CMOS process, achieve a 0.32UI timing margin and a power efficiency of 1.5pJ/bit at 10Gbps for a BER<1e-12.

Session 9 - DC DC Converters and Digital LDO's

Monday, April 15, 1:30 pm, Room 410
Session Chair: Patrick Mercier, University of California, San Diego
Session Co-Chair: Eric Soenen, TSMC

This session begins with an invited paper on advanced integrated switched-capacitor converters, then presents work on digital and analog-assisted LDOs. Two hybrid converters are then presented, and the session concludes with a fully-integrated GaN buck converter.

1:30 pm
Introduction

1:35 pm
9-1
Advanced Multiphasing: Pushing the Envelope of Fully Integrated Power Conversion (Invited), Nicolas Butzen, Michael Steyaert*, Intel, *KU Leuven

This talk discusses the main factors that have sparked the interest in monolithic power conversion and why switched-capacitor converters in particular make an excellent candidate. For this type of converter the large parasitic coupling to the substrate, the limited capacitor density on-chip, and the inherent constrained conversion ratio range, do pose a challenge. With Advanced Multiphasing, multiple out-of-phase converter cores interact with each other to arrive at a switched-capacitor converter with more than the typical two phases that in the end has more capabilities and/or better performance. Several Advanced Multiphasing techniques are discussed that focus on both high- and low-power densities, and even allow for a new type of switched-capacitor converter which has a continuously-scalable conversion ratio. Measurement results demonstrate the working principles of these techniques and show the great potential of Advanced Multiphasing in pushing the envelope of fully integrated power conversion further.

2:25 pm
9-2
A Battery-Connected Symmetric Modified Multilevel Ladder Converter Achieving 0.45W/mm^2 Power Density and 90% Peak Efficiency, Abdullah Abdulslam, Bao Huu Lam, Patrick P. Mercier, University of California San Diego

A symmetric modified multilevel ladder DC-DC converter is presented that achieves a power density of 0.45W/mm^2 and a peak efficiency of 90%. The converter supports Li-ion battery voltages via the multilevel topology that reduces the voltage swing on the inductor while topologically supporting low output resistance for low conduction losses.

2:50 pm
9-3
A Multi-Mode DC-DC Converter for Direct Battery-to-Silicon High Tension Power Delivery in 65nm CMOS, S.Chaubey, R. Harjani, University of Minnesota

The design in standard 65nm CMOS converts the Li-ion battery voltage that can vary between 4.2V to 2.8V directly to a internal VSOC voltage that ranges between 1.5V to 0.3V. The 65nm design safely handles the high voltage delivery while providing conversion ratios between 1 to 13. To maintain high efficiency throughout, the proposed DC-DC converter functions in three distinct modes - resonant, soft-switching and four-level-buck. We use a bond wire inductor = 11nH as

the high Q passive for all three modes. The design uses core devices only. The converter handles load currents between 0.5-200mA (400X), achieves a peak efficiency of 86.6% and has a peak power density of 0.3W/mm^2.

3:15 pm - BREAK

3:30 pm
9-4
Development of GaN Monolithic Integrated Circuits for Power Conversion, Yung C. Liang*,**, Ruize Sun*,**, Yee-Chia Yeo* and Cezhou Zhao***, *National University of Singapore, Singapore, **National University of Singapore (Suzhou) Research Institute, China, ***Xi'an Jiaotong-Liverpool University, China

This paper describes the development of a viable platform for the design of full GaN (Gallium Nitride) monolithic integrated circuits using the ADS (Advanced Design System) toolfor power conversion applications. A monolithic switched-mode DC-DC buck converter with integrated functional blocks and over-current protection is used to showcase the suitability of the development. The designed GaN power integrated circuit was fully fabricated and tested.

3:55 pm
9-5
A Sub-1V Analog-Assisted Inverter-Based Digital Low-Dropout Regulator with a Fast Response Time at 25mA/100ps and 99.4% Current Efficiency, Bai Nguyen, Nghia Tang, Zhiyuan Zhou, Wookpyo Hong, Deukhyoun Heo, Yangyang Tang*, Philipp Zhang*, Washington State University, *HiSilicon Technologies Corporation

To mitigate the large voltage droop caused by sub-ns dynamic current transitions in system on chips, this paper proposes a fully-integrated analog-assisted inverter-based digital low dropout regulator to obtain 160mV droop against a 25mA/100ps load step and achieve 99.4% current efficiency by using a dynamic-step quantizer and a trip-point modulator.

4:20 pm
9-6
An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Reponse, Improved PSR and Zero Minimum Load Current, M. Huang, Y. Lu*, South China University of Technology, *University of Macau

This work presents a multi-loop digital low dropout regulator (DLDO), with analog-proportional (AP) and digital-integral (DI) controls. The DI part is implemented with shift-register-based coarse-fine tuning for good output DC accuracy and fast recovery. Meanwhile, the AP part, based on an improved low-supply flipped-voltage-follower (FVF), can response fast to the load step and supply ripple. A replica loop is used to adaptively control the AP current for a sufficient dynamic current to against supply ripple, and thus further enhances the power supply rejection (PSR). When the load current is smaller than the digital least significant bit (LSB) current, the AP part takes over the LDO control. In such case, the limit cycle oscillation (LCO) is eliminated, and no longer limits the minimum load current to be zero. Implemented in a 65nm CMOS process, a 0.38ps figure of merit (FoM) and −22dB PSR at 1MHz are measured at 0.6V supply.

4:55 pm
9-7
A Charge-Pump-based LDO Employing an AC-Coupled High-Z Feedback Loop Towards a sub-4fs FoM and a 105,000x Stable Dynamic Current Range *(Outstanding Student Paper Nominee)*, Xiaoyang Wang, Patrick P. Mercier, University of California San Diego

This paper presents an event-driven charge-pump-based LDO with an AC-coupled high-Z feedback loop which achieves response(settling) time of 6.9ns(65ns), all at a 4.9µA quiescent current for a sub-4fs FoM. Thanks to the sub-Vt detecting and overflow current suppressing techniques, a 105,000x stable load range (1µA to 105mA) is obtained.

5:10 pm
9-8
Distributed Network of LDO Microregulators Providing Submicrosecond DVFS and IR Drop Compensation for a 24-Core Microprocessor in 14nm SOI CMOS, M. E. Perez, M. A. Sperling, J. F. Bulzacchelli*, Z. Toprak-Deniz*, T. E. Diemoz, IBM, *IBM T. J. Watson Research Center

A distributed network of LDO microregulators senses and corrects the voltage at multiple points on a power supply grid in a multi-core microprocessor to reduce IR drops. A switched-capacitor accelerator in each microregulator charge pump speeds up voltage transitions by 17X. Power and current efficiencies are 89.9% and 98.5%, respectively.

Session 10 - Advanced Frequency Generator

Monday, April 15, 3:30 pm, Salon D
Session Chair: Wanghua Wu, Samsung
Session Co-Chair: Woogeun Rhee, Tsinghua University

This session presents advanced frequency generator and modulation circuits. This session begins with a digitally-intensive FMCW modulator, followed by a low noise reference sampling mm-wave PLL, a 300GHZ frequency multiplier chain, and a high performance fractional-N MDLL.

3:25 pm
Introduction

3:30 pm
10-1
Digitally-Intensive Fast Frequency Modulators for FMCW Radars in CMOS (Invited), D. Cherniak, C. Samori, S. Levantino, Politecnico di Milano

Digitally-intensive PLLs have already demonstrated their effectiveness as frequency synthesizers for cellular applications, being able to fulfill the specifications in terms of phase noise, spurs and power dissipation thanks to the adoption of embedded digital processing that efficiently reduces the analog impairments. In this paper we review how these techniques further enable other capabilities, namely both wideband and linear frequency modulation. The application considered as a case study is the fast chirp generation for frequency-modulated continuous wave radar at millimeter waves. We illustrate how the combination of the two-point modulation of a digital PLL and the background digital predistortion of the DCO enable both fast and linear modulation.

4:20 pm
10-2
An mm-Wave Synthesizer with Low In-Band Noise and Robust Locking Reference-Sampling PLL, Dongyi Liao, Yucai Zhang, Zhenqi Chen*, Yanjie Wang*, Fa Foster Dai, Auburn University, *Digital Analog Integration Inc.

A two stage mm-wave frequency synthesizer with low in-band noise and robust frequency locking is presented in this paper. A type-I reference sampling PLL is utilized in the first stage to provide low in-band noise while achieving robust locking. It generates a 9GHz intermediate clock as the reference for the second stage injection locked (IL) VCO for a 4 times frequency multiplication. The chip was fabricated in a 45nm SOI CMOS technology and achieves 227fs jitter, -240dB FoM at 35.84GHz with total power consumption of 20.6mW.

4:55 pm
10-3
A 1.6-to-3.0-GHz Fractional-N MDLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 397fs Jitter at 2.5-mW Power, A. Santiccioli, M. Mercandelli, A.L. Lacaita, C. Samori, S. Levantino, Politecnico di Milano

This paper introduces a fractional-N MDLL architecture with bang-bang subsampling and reduced DTC range, achieving -244dB jitter FOM in a 0.0275mm2 core area in 65nm CMOS.

5:10 pm
10-4
A 280-325 GHz Frequency Multiplier Chain With 2.5 dBm Peak Output Power, P. Zhou, J. Chen, P. Yan, Z. Chen, D. Hou, W. Hong, Southeast University, Nanjing, China

This paper presents a single-chip 300 GHz amplifier multiplier chain in a 130 nm SiGe process. The chip shows a competitive bandwidth over 280 to 325 GHz. The measured peak output power is 2.5 dBm at 284 GHz and higher than 0 dBm from 282 to 314 GHz.

Session 11 - Panel-Can Intelligent Automation Improve Custom/Analog Design

Monday, April 15, 4:20 pm, Room 408
Session Chair: Brian J. Mulvaney, NXP
Session Co-Chair: Farhana Sheikh, Intel Circuit Research Lab

For several decades the basic design flow for analog/custom integrated circuits has not changed: schematic capture, circuit simulation, and semi-manual layout. Will this still be true twenty years from now? Is the reason for lack of progress in better design automation because the problem is 'too hard'? Or are analog designers unwilling to give up the art of design? Hardware resources for more and more simulation have never been better, but there seems to be an insatiable appetite to consume all available machines. Can a more intelligent use of resources, perhaps using rapidly developing machine learning techniques, break this bottleneck?

Panelists
Elad Alon (UC-Berkley)
Peng Li (Texas A&M University)
John Khoury (Si Lab) (TPC)
Huang-Jin Lee (Intel)
Jeff Dyck (Siemens/Mentor)

Tuesday, April 16

Session 12 - Advanced RF Techniques

Tuesday, April 16, 8:30 am, Salon D
Session Chair: Jacques "Chris" Rudell, University of Washington
Session Co-Chair: John Long, University of Waterloo

A collection of advanced RF topics for higher data-rates, automated transceiver, synthesis including a PLL, in addition to noise and interference suppression techniques.

8:30 am
Introduction

8:35 am
12-1
A 52-dB Self-Interference Rejection Receiver using RF Code-Domain Signal Processing, Ahmed Hamza, Hussam AlShammary, Cameron Hill, James Buckwalter, University of California, Santa Barbara

This paper presents a code-domain receiver for STAR applications. The RX achieves 52dB of TX rejection using DSSS techniques at the antenna. The rejection is achieved by code notch and code pass filters operating at the same frequency. The RX is tunable from 0.25GHz to 1.25GHz with 39dB of gain.

9:00 am
12-2
An HDL-described Fully-synthesizable Sub-GHz IoT Transceiver with Ring Oscillator Based Frequency Synthesizer and Digital Background EVM Calibration, Bangan Liu, Yuncheng Zhang, Junjun Qiu, Wei Deng, Zule Xu, Haosheng Zhang, Jian Pang, Yun Wang, Rui Wu, Teruki Someya, Atsushi Shirane, Kenichi Okada, Tokyo Institute of Technology

This paper presents a fully synthesizable sub-GHz IoT transceiver in 65nm CMOS with 3.3/4.6mW RX/TX power consumption. The TRX has a ring oscillator based PLL-based transmitter and a digital-intensive heterodyne receiver. It achieves 0.9% EVM and -41dB ACPR in TX mode, and -94dBm sensitivity and 36dB ACR in RX mode.

9:25 am
12-3
A Single-Channel RF-to-Bits 36Gbps 8PSK RX with Direct Demodulation in RF Domain *(Outstanding Sutdent Paper Nominee)*, Hossein Mohammadnezhad, Huan Wang, Andreia Cathelin*, Payam Heydari, University of California, Irvine, *STMicroelectronics

A single-channel 115-135GHz direct demodulation RF-to-bits 8PSK RX is presented. The output of this receiver is demodulated bits, obviating the need for power-hungry highspeed- resolutions ADCs. A novel RF-correlation-based idea is introduced to enable 8PSK direct demodulation. A max conversion gain of 32dB and min NF of 10.3dB was measured. A data rate of 36Gbps was wirelessly measured at 0.3m distance and directly demodulated with a BER of 1e-6. The measured receiver sensitivity at this BER is -41.28dBm.

9:50 am
12-4
An LPTV Noise Cancellation Technique for a 0.9-V Filtering-by-Aliasing Receiver Front-End with >67-dB Stopband Rejection, S. Bu, S. Hameed*, S. Pamarti, University of California, Los Angeles, *Silvus Technologies, Inc.

An LPTV noise cancellation technique for filtering-by-aliasing receivers is presented. It improves the NF by about 3 dB while achieving 67-dB stopband rejection with a transition bandwidth of 4× the RF BW. With an N-path filter, the IIP3 is +18 dBm and the blocker 1-dB compression point is +9 dBm.

10:15 am - BREAK

Session 13 - High Speed ADCs

Tuesday, April 16, 8:30 am, Salon E
Session Chair: Seung-Tak Ryu, KAIST
Session Co-Chair: Ayman Shabra, MediaTek

This session introduces 7 high speed ADC design techniques including novel architectures such as 7/8-way split TI ADC, SAR-based hybrid ADC, multi-bit/cycle SAR. Subranging Flash, and time-domain folding and pulse shrinking cells.

8:30 am
Introduction

8:35 am
13-1
A 10b 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration, Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei[1], R. P. Martins[2], University of Macau, Macao, [1]University of Texas at Austin, Austin, [2]On leave from Universidade de Lisboa, Portugal

This paper presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background mismatch calibration. Benefitting from the proposed split TI topology, the mismatch calibration convergence speed is fast with random signals without any extra analog circuits. A prototype 10-b 1.6-GS/s 7/8- way split TI-SAR ADC in 28-nm CMOS achieves 54.2dB SNDR at Nyquist rate with a 2.5-GHz 3-dB bandwidth, while the power consumption is 12.2mW leading to a Walden FOM of 18.2 fJ per conversion step.

9:00 am
13-2
A 280MS/s 12b SAR-Assisted Hybrid ADC with Time Domain Sub-Range Quantizer in 45nm CMOS, Zhan Su, Hechen Wang, Haoyi Zhao, Zhenqi Chen*, Yanjie Wang* and Fa Foster Dai, Dept. of Electrical and Computer Eng., Auburn University, *Digital Analog Integration, Inc.

This paper presents a SAR assisted hybrid ADC that uses a time domain quantizer for sub-range quantization. The proposed hybrid ADC utilizes an 8b 2b/c SAR coarse ADC pipelined with a 6b 2-dimensional Vernier TDC as the fine quantizer for high-resolution and high conversion rate.

9:25 am
13-3
A 10-b 320-MS/s Dual-Residue Pipelined SAR ADC with Binary Search Current Interpolator, K.-I. Cho, Y.-S. Kwak, H.-J. Kim, J.-H. Boo, S.-H. Lee, G.-C. Ahn, Sogang University

This paper presents a 10-bit 320-MS/s dual-residue pipelined SAR ADC that shares a DAC and a residue amplifier to improve the matching of two residue paths. Current interpolator based SAR ADC is employed for the second stage. The ADC in 28 nm CMOS achieves 54.0 dB SNDR at Nyquist input.

9:50 am
13-4
A 7b 2.6mW 900MS/s Nonbinary 2-then-3b/cycle SAR ADC with Background Offset Calibration, Dengquan Li, Jiaxin Liu*, Haoyu Zhuang**, Zhangming Zhu, Yintang Yang, Nan Sun*, Xidian University, *The University of Texas at Austin, **University of Electronic Science and Technology of China

This paper presents a 2-then-3b/cycle SAR ADC with background offset calibration. By exploiting comparators with two input paths, multiplication and subtraction can be performed in comparators instead of extra DAC array, resulting in reduced area and power overhead. A 7-bit prototype SAR ADC achieves 36.6fJ/conv-step FOM at 900MS/s sampling rate.

10:15 am - BREAK

10:40 am
13-5
A 3mW 6b 4GS/s Subranging ADC with Adaptive Offset-Adjustable Comparators, Chung-Ming Yang, Tai-Haur Kuo, National Cheng Kung University

This work implements a 3mW 6b 4GS/s subranging ADC in 28nm CMOS. The proposed subranging architecture is free of both conventional reference-voltage switching to increase speed and the resistor ladder to save power. At 3.6GS/s, the ADC has the best Walden FOM of 22.7fJ/conv-step compared with prior state-of-the-art ADCs.

11;05 am
13-6
A 2-way 7.3-bit 10 GS/s Time-based Folding ADC with Passive Pulse-Shrinking Cells, Mohsen Hassanpourghadi, Mike Shou-Wei Chen, University of Southern California

This paper presents a two-way time-based folding ADC that uses a passive pulse-shrinking technique to quantize time with a purely passive R-C network. The prototype is implemented in 65nm CMOS and achieves 32.5dB SNDR at Nyquist frequency with the sample-rate of 10GS/s while consuming 29.7mW, yielding an FOM of 86fJ/c-step.

11:30 am
13-7
A Generated 7GS/s 8b Time-Interleaved SAR ADC with 38.2dB SNDR at Nyquist in 16nm CMOS FinFET, Jaeduk Han, Eric Chang, Stevo Bailey, Zhongkai Wang, Woorham Bae, Angie Wang, Nathan Narevsky, Amy Whitcombe, Pengpeng Lu, Borivoje Nikolić, Elad Alon, University of California at Berkeley

This paper presents a 7GS/s time-interleaved SAR ADC produced from a generator-based design flow. Various design techniques are utilized for a compatibility with a 16nm FinFET process. The ADC layout is generated by placing elements on a grid to abstract design rules. The ADC achieves 38.2dB SNDR, consuming 45.2mW.

Session 14 - Biomedical Circuits and Systems

Tuesday, April 16, 8:30 am, Room 408
Session Chair: Kaushik Sengupta, Princeton University
Session Co-Chair: Jerald Yoo, National University of Singapore

The session focuses on state-of-the art innovations in biomedical circuits and systems ranging from cell-level analysis to neuro-modulation and wearable technology.

8:30 am
Introduction

8:35 am
14-1
Distributed Microscale Brain Implants with Wireless Power Transfer and Mbps Bi-directional Networked Communications, Vincent W. Leung, Lingxiao Cui, Sravya Alluri, Jihun Lee*, Jiannan Huang, Ethan Mok*, Steven Shellhammer**, Ramesh Rao, Peter Asbeck, Patrick P. Mericer, Lawrence Larson*, Arto Nurmikko*, Farah Laiwalla*, University of California, San Diego, *Brown University, **Qualcomm Inc.

We propose a wireless BMI system based on distributed IC implants. In order to time-multiplex the uplink data transmission, an ASK-PWM downlink data protocol was implemented. This paper presents the first experimental validation of simultaneous wireless power transfer and bi-directional RF data communications on a network of brain implant ICs.

9:00 am
14-2
A CMOS 2D Transmit Beamformer With Integrated PZT Ultrasound Transducers For Neuromodulation, Tiago Costa, Chen Shi, Kevin Tien, Kenneth L. Shepard, Columbia University

We present a CMOS 2D beamformer with integrated lead zirconate titanate (PZT) ultrasound transducers for neuromodulation of the peripheral nerves. The proposed prototype can achieve a maximum focal pressure of approximately 100 kPa with a 5 V supply at 0.5 cm depth without including an acoustic matching layer.

9:25 am
14-3
Understanding Body Channel Communication (Invited), Jaeeun Jang*, Joonsung Bae**, and Hoi-Jun Yoo*, *KAIST, **Kangwon National University

Increasing requirements of convenient and higher energy efficiency near human body gives more attention to body channel communication (BCC) technology. BCC, utilizing human body as communication medium, can take advantage of both wireline and wireless communication in body area. In this paper, several underlying key considerations of BCC would be introduced from its fundamental basis to target applications. Paper will starts from the comparison with general RF technology and BCC, and introduce historical review of BCC researches. Two analogical perspective to understand BCC and several challenges in its design will be discussed. After that, with following recent transceiver IC design trends, design efforts and their achievements would be covered. After introducing future applications that promising for BCC, this paper would be concluded.

10:15 am - BREAK

10:40 am
14-4
An 8-channel 2.1μW 0.017mm^2 0.04% Gain Mismatch Bio-potential Recording AFE using Group-Chopping Technique, Tao Tang*, Jeonghoan Park*, Lian Zhang*, Kian Ann Ng**, Jerald Yoo*,**, *National University of Singapore, **Singapore Institute for Neurotechnology

An 8-ch bio-potential recording AFE with less than 0.04% gain mismatch is presented. The proposed Group-Chopping Instrumentation Amplifier exploits group-chopping scheme to achieve the lowest gain mismatch reported to date and

improves between-channel CMRR among all channels. It consumes 2.1μW/Ch. and achieves NEF of 2.1, while occupying 0.017mm^2/Ch.

11;05 am
14-5
A 0.6-mm^2 Powering and Data Telemetry System Compatible with Ultrasound B-Mode Imaging for Freely Moving Biomedical Sensor Systems, Y. Zhang, K. L. Shepard, Columbia University

Fabricated in 180nm technology, a 0.6mm^2 57pW IC is designed to harvest power from and establish bi-directional datalink with an ultrasound B-mode imager, achieving 0.8mm data signature based localization accuracy with 71mm maximum implant depth, working towards a mm sized freely moving ingestible or implantable biomedical systems.

11:30 am Lunch

2:00 pm
Introduction

2:05 pm
14-6
A 20.1-μW 1.8-GHz Near-Field Dielectric Plethysmography (NF-DPG) Heart-Rate Sensor with Time-based Edge Sampling *(Outstanding Regular Paper Nominee)*, Jun-Chau Chien, Stanford University

This paper presents a near-field dielectric plethysmography (NF-DPG) heart-rate sensor for low-power operation. By interrogating the contracting and expanding blood vessels with GHz-frequency fringing electric fields from the on-board coplanar electrodes, pulsing heart-rate signals are detected through changing permittivity at the fingertips. The sensor employs large-signal time-based edge sampling and double-integration chopper stabilization technique to maximize the sensitivity and to minimize the flicker noise. Implemented in 0.18-μm CMOS technology, the NF-DPG heart-rate sensor consumes 20.1 μW at a 100-Hz sampling rate while achieving an RMS inaccuracy of 1.64 bpm.

2:30 pm
14-7
2D Magnetic Sensor Array for Real-time Cell Tracking and Multi-site Detection with Increased Robustness and Flow-rate, Hao Tang[1], Suresh Venkatesh[1], Zhongtian Lin[2], Xuyang Lu[1], Hooman Saeidi[1], Gulam M. Rather[3], Joseph R. Bertino[3], Chen-Yong Lin[4], Mehdi Javanmard[2], and Kaushik Sengupta[1], [1]Princeton University, [2]Rutgers University, [3]Rutgers Cancer Institute of New Jersey, and [4]Georgetown University

In this article, we present a 2D oscillator-based magnetic sensor CMOS IC for flow cytometry. The CMOS IC packaged with a microfluidic channel eliminates the need for hydro-focusing by allowing uninhibited flow over the 2D chip surface. The chip exploits multi-site detection capability allowing simultaneously high flow rate for trace cell detection, reduced false positive rates, and real-time cell tracking. We demonstrate this with a 7x7 array in 65-nm CMOS with lymphoma cancer cells.

2:55 pm
14-8
Time Domain NIRS Optode based on Null/Small Source-Detector Distance for Wearable Applications (Invited), Sreenil Saha[*], Samuel Burri[**], Claudio Bruschini[**], Edoardo Charbon[**], Frederic Lesage[*] and Mohamad Sawan[*], [*]Polytechnique Montréal, Canada, [**]École Polytechnique Fédérale de Lausanne

We present the designs of novel optode based probes integrating light detection and light-pulsing electronics in a single CMOS chip with functional blocks such as a fast pulse-laser driver and synchronized single-photon detection circuit, while exploiting the null/small source-detector distance (ns-SDD) configuration which features the highest sensitivity to deep tissue. With the perspective of simplifying the output, photon counts are accumulated in a counter on-chip and transmitted as an analog signal mimicking the signal one would get from normal linear analog photodetectors. Development of a single optode, incorporating source and detectors very close to each other within the assembly, eliminates the use of optical fibers and could yield a completely novel near infrared system (NIRS) architecture where time-domain photon-

counting approach is utilized to quantify changes in the number of photons scattering back to nearly where they came from.

3:45 pm - BREAK

Session 15 - Security, Memory and Computing

Tuesday, April 16, 8:30 am, Room 410
Session Chair: Charles Augustine, Intel Circuit Research Lab
Session Co-Chair: Shinya Kajiyama, Hitachi

This session discusses accelerator design for solving combinational problems, partial differential equations and online learning in neuromorphic processors along with an optimized SRAM PUF circuit for enabling secure chips.

8:30 am
Introduction

8:35 am
15-1
CMOS Annealing Machine: an In-memory Computing Accelerator to Process Combinatorial Optimization Problems (Invited) ***(Outstanding Invited Paper Nominee)***, M. Yamaoka, T. Okuyama, M. Hayashi, C. Yoshimura, Takashi Takemoto, Hitachi, Ltd.

A CMOS annealing machine, an in-memory computing, that is specialized to solve combinatorial optimization problems is proposed. The computing maps problems to an Ising model and solves the optimization problems by its own convergence property. We proposed a CMOS implementation of Ising computing and fabricated two prototypes of the computer. The 1st generation prototype confirmed the power efficiency is 1800-times higher than that of the conventional von-Neumann computers. The 2nd generation prototype is organized by FPGA, and used to explore its applications.

9:25 am
15-2
An SRAM-Based Accelerator for Solving Partial Differential Equations, T. Chen, J. Botimer, T. Chou, Z. Zhang, University of Michigan

We formulate the Jacobi method in a residual form to enable the mapping of a high-precision PDE solver on SRAMs. A DLL generates word line pulses and a dual-ramp single-slope converts bit line outputs. The 66.4mW 180nm test chip is demonstrated to solve PDEs at 56.9GOPS.

9:50 am
15-3
A Highly Reliable SRAM PUF with a Capacitive Preselection Mechanism and pre-ECC BER of 7.4E-10, A. Miller, Y. Shifman, Y. Weizman, O. Keren and J. Shor, Bar-Ilan University

An SRAM PUF with an internal error reduction mechanism is presented. A capacitive preselection test identifies potentially unstable cells with insufficient mismatch. An implementation in TSMC 65nm technology disqualified all unstable cells (19.7%) in 14-arrays. A highly competitive pre-ECC BER of 7.4E-10 and an energy consumption of 16fJ/bit were achieved.

10:15 am - BREAK

10:40 am
15-4
Area-Efficient Transposable 6T SRAM for Fast Online Learning in Neuromorphic Processors, J. Koo, J. Kim, S. Ryu, C. Kim, J-J. Kim, Pohang University of Science and Technology

This paper presents a 6T SRAM-based transposable synapse memory aiming to improve online learning performance of neuromorphic processors at the minimum area cost. While a custom 8T SRAM is used in the previous transposable

synapse memory, the proposed one uses 6T SRAM, which leads to substantial area savings. Based on the proposed hierarchical word line structure with row transition multiplexer, both row-wise and column-wise accesses are made possible in an integrated SRAM array. A 64K-synapse memory employing the proposed scheme is implemented in a 28nm CMOS technology with 17.7% area overhead compared to the non-transposable 6T synapse memory; 50.0% area savings compared to the transposable 8T synapse memory, and 35.5% area savings compared to the previous transposable 6T synapse memory. The estimated performance gain for online spike-timing-dependent plasticity learning using MNIST dataset is 6.7× compared to the non-transposable synapse memory.

11:05 am
15-5
On-Chip Physical Attack Protection Circuits for Hardware Security (Invited), Makoto Nagata, Takuji Miki, Noriyuki Miura, Kobe University

Hardware security, application of modern digital cryptography and authentication technologies for protecting information in electronics, involves analog functionality to avoid physical threats in operation fields. This paper introduces semiconductor integrated circuits designed for on-chip detection and disablement of malicious attempts on cryptographic devices through side-channel and fault attacks. The protection against local electromagnetic attack (LEMA) and laser fault injection attack (LFIA) are demonstrated with Silicon measurements.

Session 16 - Panel-Choices (and Consequences) for Neural Network HW and Systems

Tuesday, April 16, 10:40 am, Salon D
Session Chair: Geoffrey Burr, IBM Research -- Almaden
Session Co-Chair: Chia-Yu Chen, IBM T.J. Watson Research Center

Modern neural networks and machine learning have been generating impressive real-world results, thanks to vast quantities of training data and the massive parallelism of GPUs. There are now many design efforts seeking to implement custom hardware and systems for neural networks. Such design efforts inherently involve critical choices, each with their own consequences. Should one focus on forward-inference opportunities or training opportunities? Opportunities in the cloud or at the edge? Reducing the computational load by pruning and reduced precision makes enormous sense, but at what point do these choices affect the accuracy, the applicability of the hardware across many different workloads, and sufficient flexibility for future algorithmic developments? Similarly, the choice of batch-size forces tradeoffs between efficiency and performance. Other topics worth discussing might be how to support flexible algorithm-hardware co-design despite the long lead time of hardware, the potential role of neuromorphic non-Von-Neumann architectures, and the potential role of "spiking" neurons. In this panel, we assemble a diverse group of academic and industry professionals to share their views on these choices and consequences.

Panelists
Naresh Shanbhag, University of Illinois, Urbana-Champaign
Jae-sun Seo, Arizona State University
Alicia Klinefelter, NVIDIA
David Fick, Mythic-AI
Naveen Verma, Princeton University

Session 17 - Modeling, Reliability and Safety

Tuesday, April 16, 2:00 pm, Salon D
Session Chair: Paolo Miliozzi, Maxlinear
Session Co-Chair: Farhana Sheikh, Intel Circuit Research Lab

This session will focus on transistor modeling, design for resilient and reliable computing, and design for safety critical systems and circuits.

2:00 pm
Introduction

2:05 pm
17-1
BSIM-BULK: Accurate Compact Model for Analog and RF Circuit Design (Invited), Chetan Gupta, Ravi Goel, Yogesh Singh Chauhan, Indian Institute of Technology, Harshit Agarwal, Chenming Hu, University of California Berkeley

In this work, we present the recent and upcoming enhancements of the industry standard BSIM-BULK (formerly BSIM6) model. BSIM-BULK is the latest body referenced compact model for bulk MOSFETs having a unified core, which is developed by the BSIM group for accurate design of analog and RF circuits. The model satisfies the symmetry test for DC and AC, correctly predicts harmonic slope, and exhibits accurate results for RF and analog simulations. In order to further improve the model accuracy for transconductance (gm) and output conductance (gds), an analytical model for bulk charge effect, in both current and capacitance, is implemented. Several other advanced models are added to capture real device physics. These include: parasitic current at the shallow trench isolation edges; leakage current components in zero threshold voltage native devices; a new model for NQS to capture the NQS effects up to the millimeter wave regime; self-heating effect; and heavily halo implanted MOSFET's anomalous gm, flicker noise, and IDS mismatch. All these enhancements have been implemented to high standards of computational efficiency and robustness.

2:55 pm
17-2
Low-Swing Links with Dynamic Energy-Quality Trade-off for Error-Resilient Applications, K. R. Viveka, M. Alioto, National University of Singapore

This paper proposes the use of sub-word ranking and non-uniform swing to allow graceful energy-quality tradeoff in intra-chip communication links. The proposed techniques are demonstrated in a 28nm testchip that achieves up to 4.5X energy saving over conventional full-quality links, and up to 2.2X over approximate links at iso-quality. Conventional operation with no quality degradation is also allowed for data packets that require full quality.

3:20 pm
17-3
A Counter based ADC Non-linearity Measurement Circuit and Its Application to Reliability Testing, G. Park, M. Kim, N. Pande, P. Chiu, J. Song, C.H. Kim, University of Minnesota

In this work, we demonstrated a counter based measurement circuit for precise characterization of ADC DNL and INL. Using the proposed method, we studied short-term device instability issues in a 10-bit SAR-ADC fabricated in 65nm CMOS. Results confirm that subtle DNL shifts can be accurately measured using the proposed method.

3:45 pm - BREAK

4:00 pm
17-4
Design-For-Safety For Automotive IC Design: Challenges And Opportunities (Invited), Alessandra Nardi, Samir Camdzic*, Antonino Armato, Francesco Lertora, Cadence Design Systems, *Texas Instruments

As the automotive industry marches towards higher level of autonomous driving, new requirements, such as Functional Safety, add to the traditional design/verification/implementation flow. This paper introduces the requirements to Design-For-Safety, reviews challenges and opportunities for flow automation, and reviews commonalities and differences of the Digital and Analog/Mixed-Signal flows.

Session 18 - Innovative Wireline Techniques

Tuesday, April 16, 2:00 pm, Salon E
Session Chair: Eric Naviasky, Cadence
Session Co-Chair: Sudip Shekhar, University of British Columbia

This session presents clever circuit techniques on CDR, ADC-links and inter-package signaling. In addition, two papers revive use of transmit encoding and simultaneous bidirectional links.

2:00 pm
Introduction

2:05 pm
18-1
A 2.25pJ/bit Multi-lane Transceiver for Short Reach Intra-package and Inter-package Communication in 16nm FinFET (Invited), M. Erett, D. Carey, R. Casey, J. Hudner, K. Geary, P. Neto, Xilinx Ireland, T. Lee, M. Raj, H. Zhang, A. Roldan, B. Xu, W. Lin, Y. Frans, K. Chang, Xilinx, Inc., San Jose, CA, Hongyuan Zhao, Ping-Chuan Chiang, Haibing Zhao, Nakul Narang, Kee Hian Tan,Xilinx Singapore

A multi-lane short-reach wireline transceiver is implemented in 16nm FinFET. Leveraging a low-loss channel to design low complexity transmit and receiver circuits to minimise system power. The transceiver achieves a BER of <1e-15 over a channel with 8dB loss at 28GHz with an efficiency of 2.25pJ/bit.

2:55 pm
18-2
A 13.6-16Gb/s Wireline Transceiver with Dicode Encoding and Sequence Detection Decoding for Equalizing 24.2dB with 2.56pJ/bit in 65nm CMOS *(Outstanding Sutdent Paper Nominee)*, Yusang Chun, Tejasvi Anand, Oregon State University

An alternative strategy for communicating on bandwidth-limited wireline channels without using conventional equalizers (FFE, DFE, CTLE) is presented: dicode encoding and sequence-detection decoding. Implemented in 65nm CMOS, the proposed design approach can equalize up to 24.2dB and 21.4dB loss with 2.56pJ/bit and 2.66pJ/bit efficiency, operating at 13.6Gb/s and 16Gb/s, respectively.

3:20 pm
18-3
A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS *(Outstanding Sutdent Paper Nominee)*, Jae-Won Nam, Mike Shuo-Wei Chen, University of Southern California

An ADC-based receiver is demonstrated for NRZ/PAM4 modulation, featuring a TDC-assisted multi-bit/cycle asynchronous SAR ADC with embedded-IIR equalization filter. It re-uses the existing sampling network of 8-way time-interleaved ADCs and incorporates active Gm-C integrators to form a tunable-IIR equalizer. The prototype in 65nm CMOS achieves 2.43-pJ/b FOM using 12.8-Gbuad PAM4.

3:45 pm - BREAK

4:00 pm
18-4
A 32 Gb/s Simultaneous Bidirectional Source-Synchronous Transceiver with Adaptive Echo Cancellation in 28nm CMOS, Yang-Hang Fan, Ankur Kumar, Takayuki Iwai, Ashkan Roshan-Zamir, Shengchang Cai, Bo Sun*, Samuel Palermo, Texas A&M University, *Qualcomm

This paper presented a multi-lane source-synchronous simultaneous bidirectional transceiver that employs adaptive echo cancellation to enable 32Gb/s operation over channels with near 10dB loss.

4:25 pm
18-5
A 30Gb/s 2x Half-Baud-Rate CDR, Danny Yoo, Mohammad Bagherbeik, Wahid Rahman, Ali Sheikholeslami, Hirotaka Tamura*, Takayuki Shibasaki*, University of Toronto, *Fujitsu Laboratories

This paper presents a 2x half-baud-rate clock and data recovery technique that locks to the edge by performing 2x oversampling at half-baud-rate (every other UI). A testchip was fabricated in 28nm CMOS demonstrating a 30 Gb/s 2x half-baud-rate CDR with a Tyco 5" channel with 13.06 dB loss at Nyquist.

Session 19 - Forum-Heterogeneous Integration and Chip-to-Chip Communication

Tuesday, April 16, 2:00 pm, Room 410
Session Chair: Nikhil Shukla,
Session Co-Chair: Arijit Raychowdhury, Georgia Institute of Technology

2:00 pm
Introduction

2:05 pm
19-1
System on Package: An alternative to SoC for Heterogeneous Integration, Madhavan Swaminathan, Georgia Tech

2:30 pm
19-2
Advanced Packaging Architectures for Heterogeneous Integration, Ravi Mahajan,(Intel

2:55 pm
19-3
Chip Level Integration options using silicon Technologies for mmWave 5G Radio, Anirban Bandyopadhyay, Global Foundries

3:20 pm
19-4
Product planning, architecture, design and manufacture of a 3D-IC, Xin Wu, Xilinx

3:45 pm - BREAK

Session 20 - Panel-Research Direction Mismatches Between Industry and Academia

Tuesday, April 16, 4:00 pm, Room 410
Session Chair: David Yeh, Semiconductor Research Corporation
Session Co-Chair: Timothy O. Dickson, IBM T.J. Watson

For years, university CMOS IC design research has painted a vision and demonstrated concepts that were often deemed too risky for industry to tackle. As a result, today's industry benefits from university research in topics such as CMOS RF circuits, switched capacitor filters, and oversampled data converters, just to name a few. However, a view of today's research landscape seems to point towards a mismatch between academic research and the current IC industry. Is university research paving a sufficiently long-term roadmap, or is industry too short-term focused to notice? Can industry buy into university ideas that are proven in 65nm CMOS, but not in 14nm FinFET? What does industry value more - student talent development, or technology demonstrations with record-breaking FoM? And dare we even broach the subject of a 'funding mismatch'? Our panel of experts will dive into these topics - and many more!

Panelists
Ram Krishnamurthy, Intel
Jim Wieser, Texas Instruments
Woogeun Rhee, Tsinghua University
Pavan Hanumolu, University of Illinois, Urbana-Champaign
Shiva Gowni, NXP

Wednesday, April 17

Session 21 - Data Converter Techniques

Wednesday, April 17, 8:30 am, Salon D
Session Chair: Yunzhi Dong, Analog Devices

Session Co-Chair: Delong Cui, Broadcom

This session presents clever circuit techniques on CDR, ADC-links and inter-package signaling. In addition, two papers revive use of transmit encoding and simultaneous bidirectional links.

8:30 am
Introduction

8:35 am
21-1
A 40/30 MS/s Dual-Mode Pipelined ADC with Error Averaging Techniques in 90nm CMOS Achieving 71.2/74.5 dB SNDR over the Entire Nyquist Bandwidth, Tsung-Chih Hung, Tai-Haur Kuo, National Cheng Kung University

This work presents two capacitor mismatch error reduction techniques, sorted-capacitor averaging (SCA) and two-phase averaging (TPA), combined with the finite opamp gain error reduction technique, averaging correlated level shifting (ACLS). Operating with SCA/TPA at 40/30MSPS with Nyquist inputs, the ADC achieves 71.2/74.5dB SNDR, 46.3/40.0fJ/conversion-step Walden Figure-of-Merit and 166.8/169.1dB Schreier Figure-of-Merit.

9:00 am
21-2
A 4MS/s 10b SAR ADC with integrated Class-A buffers in 65nm CMOS with near rail-to-rail input using a single 1.2V supply, Harijot Singh Bindra*, Anne-Johan Annema*, Simon M. Louwsma**, Gerard Wienk*, Bram Nauta*, *University of Twente, **Teledyne DALSA

We present a 10b 4MS/s differential-input SAR ADC with integrated Class-A input buffers. Thanks to a signal range dependent swapping circuit, both buffers only need to handle either the upper or lower half of the full-scale input range. This enables operation of buffers and ADC at a single 1.2V supply while still providing near rail-to-rail operation. With a lowest reported (ADC + buffer) Walden FoM of 87fJ/conv-step it is an excellent choice for low power IoT applications.

9:25 am
21-3
A 0.9V, 79.7dB SNDR, 2MHz-BW Highly linear OTA-less 1-1 MASH VCO-based ∆Σ ADC with a Novel Phase Quantization Noise Extraction Technique *(Outstanding Sutdent Paper Nominee)*, H. Maghami*, P. Payandehnia*, H Mirzaie*, R Zanbaghi**, S. Dey*, J. Goins*, K. Mayaram*, T. S. Fiez***, *Oregon State University, **Cirrus Logic Inc, ***University of Colorado

A highly linear OTA-less 1-1 MASH VCO-based ADC is presented. The quantization noise of a multi-phase VCO-based quantizer is extracted in the time domain as a PWM signal using a novel technique. The prototype achieves DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7dB over 2MHz BW. The fabricated design consumes 1.248mW with FOMs of 171.7dB.

9:50 am
21-4
A 12 MHz BW, 80 dB SNDR, 83 dB DR, 4th order CT-ΔΣ modulator with 2nd order noise-shaping and pipelined SAR-VCO based quantizer, S. Dey, K. Mayaram, T. Fiez*, Oregon State University, *University of Colorado, Boulder

A 2nd-order noise-shaping, high-linearity, SAR-VCO based quantizer is proposed. The SAR and VCOQ operate in a pipeline to reduce quantizer delay. Quantization error leakage due to VCO gain variations gets noise-shaped. By using this quantizer in a 2nd-order ΔΣ loop, 4th-order noise shaping is achieved using two OTA-RC integrators.

10:15 am - BREAK

10:40 am
21-5
A 2MHz BW Buffer-Embedded Noise-Shaping SAR ADC Achieving 73.8dB SNDR and 87.3dB SFDR, Taewoong Kim, Youngcheol Chae, Yonsei University

This paper presents a buffer-embedded noise-shaping SAR ADC, that achieves significant power saving by separating the capacitive DAC and the sampling capacitor. Implemented in a 65nm CMOS, the ADC achieved 73.8dB SNDR, 77dB DR, and 87.3dB SFDR in 2MHz bandwidth without calibration, while consuming only 2.13mW including the input buffer.

11:05 am
21-6
A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique, Xiyuan Tang*, Yi Shen**, Linxiao Shen*, Wenda Zhao*, Zhangming Zhu**, Visvesh Sathe***, and Nan Sun*, *University of Texas at Austin, **Xidian University, ***University of Washington

This paper presents a 10-bit 120MS/s SAR ADC. A novel reference ripple cancellation technique is proposed to address the reference settling issue during high-speed DAC switching. Instead of consuming power/area to ensure a fast recovery or small ripple, it provides a feed-forward path for the reference ripple and performs cancellation at the comparator input, thus guaranteeing a ripple-free signal. A 5-bit dedicated DAC is configured to emulate the ripple transfer function of the main DAC. A 40nm CMOS prototype achieves a Walden FoM of 15fJ/c-s while requiring only 3pF decoupling capacitor

11:30 am
21-7
A 60-fJ/step 11-ENOB VCO-based CTDSM Synthesized from Digital Standard Cell Library, Shaolan Li, Biying Xu, David Z. Pan, Nan Sun, The University of Texas at Austin

Synthesizable ADCs are economically attractive as they enable low-cost rapid development of SoC; however, they are yet to achieve adequate performance to meet practical application specs. This paper presents a fully synthesized VCO-based ΔΣ modulator that built solely from digital standard cells and a few resistors. Leveraging time-domain techniques, the design is robust against circuit and layout imperfections, thus enabling a simple hierarchy-less synthesis approach without sacrificing performance. Fabricated in 40-nm CMOS, the prototype occupies only 0.01 mm2. It achieves 68.8 dB SNDR over 4-MHz BW while consuming 1.08 mW, displaying 60-fJ/step Walden FoM that matches with state-of-the-art manual-designed CTDSMs.

11:55 am
21-8
A 20 kHz Bandwidth Resistive DAC with 135 dBA Dynamic Range and 125 dB THD, A. Shabra, P. Cooney, A. Cantoni, J. Bamford, S. Ho and M. Ashburn, MediaTek

We present a FIR R-DAC with a low distortion output routing method and a current output reference. It combines vector element selection and fixed transitioning of elements to suppress mismatch and ISI. A 40nm CMOS prototype has a measured dynamic range of 135dBA, a -124.5dB THD+N, and a -125dB THD.

Session 22 - Sensors and Integrations

Wednesday, April 17, 8:30 am, Salon E
Session Chair: Steven Bowers, University of Virginia
Session Co-Chair: Arijit Raychowdhury, Georgia Institute of Technology

This session starts begins with 3 papers on sensors, from THz imaging to biosensors and dosimeters. It continues with a flexible substrate ADC and concludes with 3D integration

8:30 am
Introduction

8:35 am
22-1
Fully Integrated Solutions for High Resolution Terahertz Imaging (Invited) ***(Outstanding Invited Paper Nominee)***, Ali Mostajeran*, Hamidreza Aghasi**, S. M. Hossein Naghavi***, Ehsan Afshari***, *Qualcomm Atheros Inc., **Acacia Communications, ***University of Michigan

This paper is an overview of the advances of the integrated sub-THz/THz imaging technology. The challenges to implement fully integrated imaging systems at this frequency range are discussed and solutions to overcome them are presented. We review a coherent phased locked imaging system, a FMCW radar at 170GHz and a FMCW radar at 220 GHz with a state-of-the-art radiation bandwidth of 62GHz. We also demonstrate the Inverse Synthetic Aperture Radar (ISAR) technique with a fully integrated THz imaging system in order to reconstruct high resolution 2D and 3D images. Finally, we conclude the paper by suggest emerging methods for a real-time THz imaging.

9:25 am
22-2
A Microwave-Optical Biosensor with 5.4ppm Label/Reference-free Long-term Stability and Single Photon Sensitivity in 28nm Bulk CMOS, L. Zhang, A. Ameri, M. Anwar*, A. M. Niknejad, University of California Berkeley, * University of California San Francisco

A hybrid microwave and optical biosensor is presented. The microwave sensing unit is a superharmonic coupled QVCO for permittivity detection which achieves label/reference-free 5.4ppm 8-hour stability. The optical sensing unit is an SPAD array for photon counting, which implemented in 28nm bulk CMOS for the first time.

9:50 am
22-3
A 2-in-1 Temperature and Humidity Sensor Achieving 62 fJ·K^2 and 0.83 pJ·(%RH)^2, Haowei Jiang, Chih-Cheng Huang, Matthew Chan, Drew A. Hall, University of California San Diego

This paper presents the first reported CMOS 2-in-1 temperature and humidity sensor consisting of a unified R&C-to-T converter. Using a frequency-locked-loop with an incomplete-settling switched-capacitor-based Wheatstone bridge and a time-to-digital converter, it achieves a state-of-the-art humidity sensitivity FOM and has low energy (15.6 nJ/meas.) suitable for IoT applications.

10:15 am - BREAK

10:40 am
22-4
A Wearable Real-time CMOS Dosimeter with Integrated Zero-bias Floating-Gate Sensor and an 861nW 18-bit Energy-Resolution Scalable Time-based Radiation to Digital Converter *(Outstanding Sutdent Paper Nominee)*, Baibhab Chatterjee, Charilaos Mousoulis, Shovan Maity, Anurag Kumar, Sean Scott*, Daniel Valentino*, Dimitrios Peroulis, and Shreyas Sen, Purdue University, *Landauer Inc.

The first monolithic CMOS radiation dosimeter is presented which consists a floating-gate resistive sensor (sensitivity =14Ω/Rad), and a time-based resistance-to-digital-converter (RDC: 18-bit, 861nW power @100S/s, 3.29pJ/conversion-step energy-efficiency). The time-based RDC exhibits in-field resolution-energy scalability by controlling the total integrated time for measurement, achieving 6-bit better resolution than state-of-the-art VCO-based designs.

11:05 am
22-5
Flexible 16nJ/c.s. 134S/s 6b MIM C-2C ADC using Dual Gate Self-aligned Unipolar Metal-Oxide TFTs, N. Papadopoulos, S. Steudel, M. Ameys, K. Myny, imec, A.J. Kronemeijer, Holst Center

A unipolar 6bit SAR C-2C ADC fabricated on 15um thick flexible substrate is demonstrated. The ADC is operated at a clock speed of 2kHz and achieves FoM=16.58nJ/c.s. (40% lower than state-of-art) in a threefold smaller footprint using dual gate self-aligned TFT on polymeric substrate.

11:30 am
22-6
Three-dimensional Integration (3DI) with Bumpless Interconnects for Tera-scale Generation ~ High Speed, Low Power, and Ultra-small Operating Platform (Invited), Koji Sakui[1,2], Takayuki Ohba[1], [1]Tokyo Institute of Technology, FIRST, WOW Alliance, [2]Honda Research Institute Japan Co., Ltd.

The prospect of three-dimensional (3D) integration for Terabyte large scale integration using bumpless interconnects with low-aspect-ratio TSVs and ultra-thinning are discussed. Bumpless (no bump) interconnects between wafers are a second-generation alternative to the use of micro-bumps for Wafer-on-Wafer (WOW) technology. Ultra-thinning of wafers down to 4μm provides the advantage of a small form factor, not only in terms of the total volume of 3D ICs, but also the aspect ratio of Through-Silicon-Vias (TSVs). The bumpless interconnects technology can increase the number of TSVs per chip with fine pitch of TSVs, and reduce the impedance of the TSV interconnects with no bumps. Therefore, a promising operating platform with a higher speed by enhancing parallelism, lower power by no bumps, and smaller size by thinning wafers, can be realized.

Session 23 - Emerging Power Management Techniques and Energy Harvesting

Wednesday, April 17, 8:30 am, Room 408
Session Chair: Stefano Pietri, NXP
Session Co-Chair: Mehdi Kiani, Pennsylvania State University

Novel circuit techniques for emerging power management and efficient vibration, thermal and solar energy harvesting will be presented in this session.

8:30 am
Introduction

8:35 am
23-1
A Sub 1μW Switched Source + Capacitor Architecture Free of Top/Bottom Plate Parasitic Switching Loss Achiving Peak Efficiency of 80.66% at a Regulated 1.8V Output in 180nm, M. Megahed*, Y. Ramadass** and T. Anand*, *Oregon State University, **Kilby Labs, Texas Instruments

This paper presents a switching approach that helps to break the trade-off between the charge redistribution loss and top/ bottom plate switching loss in a switched capacitor harvester. The top/bottom plate switching loss is eliminated and charge redistribution loss is reduced to achieve 80% efficiency while harvesting 1μW power.

9:00 am
23-2
An 83mA 96.8% Peak Efficiency 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation, Wen Chuen Liu, Pei Han Ng*, Robert Pilawa-Podgurski, University of California at Berkeley, *University of Illinois at Urbana-Champaign

An auto-capacitor-balancing pulse frequency modulation controlled 3-level boost converter is implemented in low-voltage process (65nm CMOS) for continuous high step-up power conversion with full-range Vout regulation and embedded capacitor balancing. This converter achieves >7X step-up conversion and 96.8% peak efficiency, operating from 0.3-3.0Vin to 2.4-5.0Vout with 83mA peak output current.

9:25 am
23-3
A Low Cost 100 MHz 2-Stage PSiP and Evolution to a Co-Packaged/Fully-Integrated Voltage Regulator for SoC Power Delivery (Invited), James T. Doyle, Jonathon C. Stiff, Santosh KulkAysel Yildiz, Yemi Omole, Kevin Chang, Dialog Semiconductor

A self-contained power delivery system in a SiP package or co-packaged in an SoC POP for CPU and GPU cell phone application is presented. State of the art performance is achieved utilizing a low-cost high voltage (5 V/1.3 V) process (0.13 μm BCD). This allows either a 2-stage or single-stage combined version on the same die. The path towards fully integrated power supply on SoC chip or co-packaged is described with results. On-going methods and options for realizing integrated or co-package inductors are being developed simulated and fabricated with results provided. Initial results of a stage 2, 100 MHz PSiP are also included with fast DVS results (>1 V/μs). Transient response and settling of less than 100 ns, consistent with 10 MHz bandwidth, were also obtained. Advantages of a 0.13 μm process include lower cost per

unit area, lower leakage, increased dynamic range, more accurate and lower power references. Performance results are superior to other stage 2 results reported using more advanced CMOS process technology nodes (28 nm and 14 Trigate) and at a lower cost. Evolution to a fully integrated high performance 2-stage design is presented with simulated and measured results.

10:15 am - BREAK

10:40 am
23-4
A Monolithic I^2V^2-Controlled Dual-Phase LED Matrix Driver for Automotive Adaptive Driving Beam (ADB) Headlighting, Yong Qu, Wei Shu, Joseph S. Chang, Nanyang Technological University

This paper presents a monolithically realized I2V2-controlled dual-phase LED matrix driver featuring high power-efficiency (94.8%) and substantially small LED current-ripple factor (5%). Attributed to the proposed I2V2 controller, accurate LED current regulation and fast transient response are achieved.

11:05 am
23-5
A 17V-to-45V Input 25µW-to-10mW Output Power, 90.2%-Peak-Efficiency SC DC-DC Converter with Recursive Output Connection for High-Voltage Energy Harvesting, Hassan Saif, Muhammad Bilawal Khan, Yoonmyung Lee, Sungkyunkwan University, South Korea

A new recursive output connection switched-capacitor (SC) DC-DC converter for high-voltage harvesters is proposed in this paper. The novel architecture of the recursive output connections in each SC stage significantly reduces the conduction loss, which is the dominant loss in cascaded SC converters for low conversion ratios. Four configurable-ratio SC stages are connected through configurable series/parallel stage interconnect, which provides a wide range of harmonic conversion ratios ranging from 1/3 to 1/13. The proposed SC converter is fabricated in 0.35µm high-voltage CMOS process, achieving efficient operation over an input voltage range of 17V to 45V and wide output power range of 25µW to 10mW with peak efficiency of 90.2%. Load and line regulation is provided by a two-step controller, which periodically tracks the optimal conversion ratio and switching frequency.

11:30 am
23-6
A 3.5 mV Input, 82% Peak Efficiency Boost Converter with Loss-Optimized MPPT and 50 mV Integrated Cold-Start for Thermoelectric Energy Harvesting, S. Bose, T. Anand, M.L. Johnston, Oregon State University

An 82% peak efficiency single-inductor boost converter is presented that can sustain operation with a minimum Vin of 3.5mV by means of a loss-optimized MPPT scheme. The converter can self-start at 50mV using an on-chip cold-start mechanism and is suitable for battery-less thermoelectric energy harvesting using human body heat.

1:35 pm
23-7
Low-Cost Fully Autonomous Piezoelectric Energy Harvesting Interface Circuit with up to 6.14x Power Capacity Gain, B. Çiftci, S. Chamanian, H. Uluşan, H. A. Yiğit, A. Koyuncuoğlu*, A. Muhtaroğlu**, H. Külah, METU, *METU-MEMS, **METU-NCC

This paper presents a novel fully autonomous interface using a new energy extraction technique called Synchronized Switch Harvesting on Capacitor-Inductor to extract energy from environmental vibrations. The circuit provides maximum of 90.1% conversion efficiency and 6.14x the maximum output power of an ideal full-bridge rectifier by employing a 68µH inductor.

2:00 pm
23-8
A 1–10MHz Frequency-Aware CMOS Active Rectifier with Dual-Loop Adaptive Delay Compensation and >230mW Output Power for Capacitively Powered Biomedical Implants, R. Erfani, F. Marefat, P. Mohseni, Case Western Reserve University

This paper presents a frequency-aware CMOS active rectifier with dual-loop adaptive delay compensation and automatic adaptation to the input frequency for capacitively powered biomedical implants with high power budgets.

Session 24 - Forum-Alternative Computing Models using Analog/MS Computational Substrates

Wednesday, April 17, 8:30 am, Room 410
Session Chair: Siddharth Joshi,
Session Co-Chair: Shreyas Sen, Purdue University

8:30 am
Introduction

8:35 am
24-1
Shannon-inspired Deep In-memory Computing, Naresh Shanbag, UIUC

9:00 am
24-2
Memory-Efficient Neuromorphic Learning and Inference, Gert Cauwenberghs, University of California, San Diego

9:25 am
24-3
Compute-in-Memory with SRAM Technologies, Shimeng Yu, Georgia Institute of Technology

9:50 am
24-4
In-Memory Computing: All-Analog to Bit-Serial, Dennis Sylvester, University of Mich

10:15 am - BREAK

Session 25 - Forum-Designing Secure HW

Wednesday, April 17, 10:35 am, Room 410
Session Chair: Carlos Tokunaga, Intel Corporation
Session Co-Chair: Farhana Sheikh, Intel Circuit Research Lab

10:35 am
Introduction

10:40 am
25-2
Cryptographic Circuit Primitives for Security Workloads in High-Performance Microprocessors, Sanu Mathew, Intel

11:05 am
25-2
Challenges in PUF design, Mudit Bhargava, ARM

11:30 am
25-3
Physical Security and Side-Channel Attacks, Michael Orshansky, UT Austin

11:55 am

25-4
State-of-the-Art and Challenges in Design-for-Anti-Counterfeit, Domenic Forte, University of Florida

Session 26 - RF/mmW VCOs and Mixers

Wednesday, April 17, 1:30 pm, Salon D
Session Chair: Jane Gu, University of California Davis
Session Co-Chair: Yanjie Wang, Intel Circuit Research Lab

This RF/mmW VCO session has four papers. It starts from an invited paper featuring magnetic-tuning techniques, then followed by two high frequency mm-wave VCOs. The last paper is low supply voltage and low flicker noise RF VCO.

1:30 pm
Introduction

1:35 pm
26-1
Magnetic-Tuning Millimeter-Wave CMOS Oscillators (Invited), X. Liu, Z. Huang*, J. Yin**, H. C. Luong, Hong Kong University of Science and Technology, *Samsung Semiconductor, **University of Macau

This paper presnets three prototypes to demonstrate that magnetic tuning can be employed either as coarse tuning or fine tuning or both for mm-Wave fundamental oscillators to achieve ultra-wide frequency tuning range and low phase noise.

2:25 pm
26-2
A Compact 275 GHz Harmonic VCO with -2.6 dBm Output Power in a 130 nm SiGe Process, Somayeh Khiyabani, Hamid Khatibi, Cornell University, Ehsan Afshari, University of Michigan

This paperpresents a new method for high frequency harmonic VCO design. A capacitive degeneration is employed to shape the output conductance (Gout) of the cross coupled structure to increase the possible oscillation frequency in addition to output power. An inductive feedback is utilized to provide large voltage swing at the input of the transistors to boost harmonic generation. Finally, the passive components at the collector improves the delivery of generated harmonic current to the load in addition to setting the oscillation frequency. Using this method, a 275 GHz harmonic VCO is designed and implemented in a 130 nm SiGe process. The measurement results show -2.6 dBm peak output power, 1.1% dc-to-RF efficiency, 3.3 % tuning range (270.3 GHz to 279.3 GHz). The chip area excluding the pads is 0.022 mm2 which results in 25 mW/mm2 power per area and 50 %/mm2 efficiency per area which is highest among reported SiGe/CMOS oscillators working above 0.75 fmax.

2:50 pm
26-3
A 219-to-238-GHz Coupled Standing-Wave VCO with 3.4-dBm Peak Output Power in 65nm CMOS, H. Jalili, O. Momeni, University of California, Davis

In this paper, we present a 0.23-THz harmonic VCO based on coupled standing wave oscillators. The transistors with drain inductances (realized by transmission lines) provide the necessary loss compensation for oscillation. At the same time, the drain transmission lines direct the output second harmonic power to the pad, thus minimizing the routing losses for the high frequency output power. Furthermore, they couple the neighboring oscillators, forcing them to oscillate out-of-phase, canceling the large fundamental frequency as well as other odd harmonics while generating in-phase second harmonics. This makes for a compact structure that minimizes the losses of the passive network by avoiding extra coupling and routing elements. The standing wave nature of the oscillators allows us to use bias as frequency tuning control and employ the transistors to play a double role as active varactors as well. We therefore avoid the undesired varactor loss and achieve a wide bandwidth of operation with reasonable variation in the output power. The chip was fabricated in a 65nm CMOS process and provides 219-to-238 GHz frequency (8.35% tuning range) with 3.4 dBm maximum output power and -105.8 dBc/Hz phase noise (at 10-MHz offset) while consuming 195 mW from a 1.5-V supply.

3:15 pm
26-4
A 0.3 V, 35 % Tuning-Range, 60 kHz 1/f^3-Corner Digitally Controlled Oscillator with Vertically Integrated Switched Capacitor Banks Achieving FoM_T of -199 dB in 28-nm CMOS, J. Du, Y. Hu, T. Siriburanon, R. B. Staszewski, University College Dublin

We present a sub-mW ultra-low-voltage (ULV) digitally controlled oscillator (DCO) with vertically integrated switched capacitor banks under a transformer for area reduction. Exploiting a passive gain of the proposed transformer improves the DCO start-up. The reduced current conduction angle in this DCO has been proved to be an effective way in suppressing flicker noise upconversion while keeping wide tuning range (TR). Implemented in 28-nm CMOS, the proposed DCO achieves -95 dBc/Hz and -118 dBc/Hz at 100 kHz and 1 MHz offsets, respectively. The TR is 35% from 2.02 GHz to 2.87 GHz. This results in a figure-of-merit with normalized TR (FoMT) at 100 kHz and 1 MHz offsets of -196 dB and -199 dB, respectively, which is a record among <0.6 V and <1 mW oscillators.

3:40 pm
26-5
A Low Power Sub-harmonic Self-Oscillating Mixer with 16.8dB conversion loss at 310GHz in 65nm CMOS, Yukun Zhu*,**,***, Hao Wang**, Kai Kang*, and Omeed Momeni**, *University of Electronic Science and Technology of China, **University of California, Davis, ***University of Texas, Dallas

A 310GHz sub-harmonic self-oscillating mixer with on-chip LO generation is demonstrated. With the large fundamental LO swings in oscillator, bulky multiplier chain and DC power consumption is saved. The achieved conversion loss (16.8dB) and noise figure (21.3dB) is the lowest among active mixers and comparable to passive mixers at 310 GHz.

Session 27 - Circuits and Systems for Security

Wednesday, April 17, 1:30 pm, Salon E
Session Chair: Shreyas Sen, Purdue University
Session Co-Chair: Zhengya Zhang, University of Michigan

This session starts with a general overview of advanced security primitives and systems followed by new designs of crypto-engines and PUFs.

1:30 pm
Introduction

1:35 pm
27-1
A 55nm 50nJ/encode 13nJ/decode Homomorphic Encryption Crypto-Engine for IoT Nodes to Enable Secure Computation on Encrypted Data, I.Yoon, N.Cao, A.Amaravati, A.Raychowdhury, Georgia Institute of Technology

We present a 55nm test-chip prototype of a crypto-system (encryption and decryption) implementing Homomorphic Encryption that can enable computation on encrypted data.Test-chip measurements show 50nJ/encode and 13nJ/decode thus making the cryptosystem suitable for sensor-nodes and IoT applications.

2:00 pm
27-2
A Metal-Via Resistance Based Physically Unclonable Function with 1.18% Native Instability, B. Park, M. Tehranipoor, D. Forte, N. Maghari, University of Florida

This paper presents a physically unclonable function (PUF) that leverages the parasitic resistance created by metal-via interconnection. An incremental analog-to-digital converter is implemented for precise measurement of the PUF. The fabricated PUF achieves a native instability of 1.18% and a distance ratio between intra-die and inter-die Hamming Distance of 314X.

2:25 pm

27-3
Enabling Ubiquitous Hardware Security via Energy-Efficient Primitives and Systems (Invited), Massimo Alioto, Sachin Taneja, National University of Singapore

Security down to hardware (HW) has become a fundamental requirement in highly-connected and ubiquitously deployed systems, as a result of the recent discovery of a wide range of vulnerabilities in commercial devices, as well as the affordability of several attacks that were traditionally considered unlikely. In large-scale networks of connected devices, attacks need to be counteracted at low cost down to individual nodes, which need to be identified or authenticated securely, and protect confidentiality and integrity of the data that is sensed, stored, processed and wirelessly exchanged. This paper provides a fresh overview of the fundamentals, the design requirements and the state of the art in primitives for HW security. Challenges and future directions are discussed using recent silicon demonstrations as case studies.

3:15 pm
27-4
A 225-950mV 1.5Tbps/W Whirlpool Hashing Accelerator for Secure Automotive Platforms in 14nm CMOS, V. Suresh, S. Satpathy, R. Kumar, M. Anders, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, S. Mathew, Intel Corporation

A Whirlpool cryptographic hashing hardware accelerator targeted for automotive security is fabricated in 14nm tri-gate CMOS with 640MHz operation and throughput of 33Gbps, measured at 750mV, 25C. Pre-addition of key and message with delayed round computation, Galois Field arithmetic optimized Sbox and multiply-less Galois Field scaling with fused reduction results in 23% area reduction compared to a conventional LUT-based design. Fully-combinational Sbox implementation enables robust sub-threshold operation down to 225mV, with a peak energy efficiency of 1.5Tbps/W measured at 250mV.

Closing and Awards Ceremony
Wednesday, April 17, 3:30 pm - 4:30 pm, Salon D

General Information

LOCATION
Hilton Austin
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Payment of the Technical Session registration fee entitles the registrant to entrance to the Sunday Educational Sessions and the Monday-Wednesday Technical Sessions, Monday's Welcome Reception, Tuesday's Conference Reception, and to one copy of the flash drive of the technical papers.

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If you have questions on your registration, please contact: By email: j.teehan@ieee.org, By phone: +1 732 465 6496

Onsite Registration and Advance Registration Badge Pick-Up
The Registration Center, located in the Salon DE Foyer, will be open as follows:

Sunday, April 14	7:00 am - 5:00 pm
Monday, April 15	7:30 am - 5:00 pm
Tuesday, April 16	8:00 am - 5:00 pm
Wednesday, April 17	8:00 am - 11:00 am

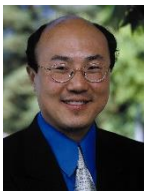
WELCOME RECEPTION AND CONFERENCE RECEPTION
Welcome Reception – Monday Evening, April 15, 5:30 pm - 7:00 pm, Salon C. The first CICC social event this year is the Welcome Reception. All conference attendees are cordially invited!

Conference Reception – Tuesday Evening, April 16, 5:30 pm – 7:30 pm, Salon C. Join the CICC for a Tuesday night reception.

IEEE SSCS Young Professionals and Women in Circuits Mentoring Event
In conjunction with the Custom Integrated Circuits Conference 2019 (CICC), the Solid-State Circuits Society (SSCS) will be holding a Young Professionals & Women in Circuits Mentoring Event. The event will be held on Tuesday, April 16 at 4:30 pm – 6:00 pm in Room 406 at the Hilton Austin in Austin, TX.

BEST PAPER POSTER DISPLAY
Wednesday, April 17 from 2:30 pm – 4:30 pm visit the posters of the best paper nominees of the 2019 CICC.

CICC KEYNOTE LUNCHEON
Tickets for the luncheon are for sale at the Registration Desk
Tuesday, 12:00 pm, April 16
Salon C



Tom Lee, Stanford University
Title: Data is the New Oil, Silicon is the New Steel: The Chimerical Internet of Everything

Abstract: To paraphrase Mark Twain, history rhymes even if it does not repeat. Listening to the rhymes of the history of wireless suggests a new verse, in which a trillion objects are connected to each other, and to us. The virtual pipes of this terascale network will carry data every bit as valuable and transformative as oil in the 20th century. But a trillion is an almost inconceivably large number, and many scaling barriers must be overcome to make a terascale future possible. This talk will decrypt the rhymes, identify the most serious impediments to scaling, and explain why silicon's evolution rhymes with that of steel, and why the Internet of Everything will be a chimera.

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