IEEE CICC Call for Papers

Submission Deadline is extended to 11:59 pm PT on November 15, 2018

IEEE Custom Integrated Circuits Conference (CICC)

is sponsored by the IEEE Solid-State Circuits Society
and technically co-sponsored by the IEEE Electron Devices Society

April 14 – April 17, 2019 at Austin Hilton, Austin, TX

Submission of original unpublished work in following areas:

Analog Circuits and Techniques for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.

Power Management circuits and design techniques including DC-DC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.

Data Converters including ADCs, DACs, time-to-digital converters, digital-to-time converters, and frequency-to-digital converters of all types enabled by new techniques, architectures, or technologies.

Wireless Transceivers and RF/mm-Wave Circuits and Systems for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.

Wireline and Optical Communications Circuits and Systems for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Design Foundations for novel digital, analog, mixed-signal, and memory circuit techniques for emerging applications such as deep learning, autonomous vehicles, IoT, security, intelligent robotics, and quantum computing. Modeling and simulation of advanced CMOS (FinFET, UTTB-SOI) and beyond-CMOS devices such as MEMS, GaN, Non-Volatile Memories, STT to improve design quality, efficiency, and reliability. Design for manufacture, test, aging, security, and reliability (novel DFT circuits and system-level testing). High-level system modeling, digital/analog design infrastructure, and verification for complex SoCs.

Emerging Technologies, Systems, and Applications
Emerging technologies solicit hardware focused papers in the technologies of tomorrow extending from new device and memory technology to system integration, applications and packaging with focus on, but not limited to:

- **Hardware-based artificial intelligence and security.** Hardware designs for emerging algorithms, hardware security, hardware- and energy-efficient artificial intelligence, machine learning, neural networks, deep learning accelerators. Applications include autonomous transportation and cloud computing.
- **Next-generation devices, technology, integration and packaging** including nano-primitives, non-silicon based technology, MEMS, emerging memories, non-traditional circuits, mm-wave/THz passives and integration, flexible, printed, large-area and organic electronics. system in package, 2.5D, 3D and monolithic 3DIC, multi-die heterogeneous integration, silicon photonic interconnects and packaging, advanced assembly and bonding, embedded cooling technologies,
- **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

Conference Technical Sessions and Events

Technical Sessions addressing a broad range of circuits, applications, design techniques, tools, test, reliability, and emerging technologies, and providing education on new, state-of-the-art developments is the core of the CICC technical program.

Educational Sessions instructed by recognized invited speakers who are among the best in the industry are included in the conference. They are valuable opportunities to refresh key skills in traditional circuit-design methods and acquire knowledge in vital new areas in analog, digital, and RF integrated circuit design.

Panels, ***Forums*** and a ***Plenary Session*** provide a platform for leaders from the IC industry and academia to present highlights on new field of research and development related to circuit design and to debate key issues and controversial topics. CICC panels are well known for their lively and thought-provoking discussion and audience participation.

Our ***Exhibit***, is where semiconductor manufacturers, IP providers, SW tool suppliers, design-service houses, and technical book publishers offer of their products. Our ***Welcome Reception***, ***Conference Luncheon*** and ***Exhibit*** with food and beverage, provide additional opportunities for discussion and peer networking.

Paper Submission

Papers can be **3~4 pages** in length with no preference on the length of the papers for review. Papers should be camera-ready and submitted electronically in PDF format using the CICC website (www.ieee-cicc.org). **Blind review will be adopted this year. Please follow the instructions given at the submission website to submit a blind version for review and a complete version for publication.** Appropriate company and government clearances MUST be obtained prior to submission. Papers must report an **original unpublished work** and concisely explain how the state-of-the-art is advanced, including results. Circuit-design papers must include measured experimental results that substantiate performance claims. **Deadline for paper submission is extended to 11:59 pm Pacific Time on November 15, 2018.** Authors of accepted papers will be notified by email by **January 20, 2019**. Top-rated papers will be invited to a special issue at ***IEEE Journal of Solid State Circuits***.

For more information, please visit www.ieee-cicc.org.

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