

Technical Program

Session 1 – Plenary Session

Monday, April 9, 8:00 am, Great Room 4/5

8:00 am **Welcome and Opening Remarks:** Kimo Tam, Analog Devices, General Chair
Alessandro Piovaccari, Silicon Labs, Conference Chair

Award Presentations

Keynote Speaker Introduction: Alessandro Piovaccari, Silicon Labs, Conference Chair



KEYNOTE SPEAKER:

Mark Pinto: CEO Blue Danube Systems

Title: Massive MIMO Active Antenna Arrays for Advanced Wireless Communications, Mark Pinto and Mihai Banu

Massive MIMO (Ma-MIMO) systems are widely expected to be a central component of future wireless networks. Using arrays of programmable radio elements, all Ma-MIMO systems attempt to shape RF energy and improve user throughput and overall system capacity by increasing SNIR and reusing spectrum between separated users. While the shape optimization process is often referred to as “beam-forming”, most Ma-MIMO systems proposed to date for sub-6 GHz cellular bands do not actually form true beams, rather a large number of radio chains and

digitizers are used to generate RF peaks and nulls based on user channel estimates. In this process, excess energy can spill into places outside the targeted users, causing unwanted interference at cell edges and wasting the available RF transmit power.

Prior to onset of Ma-MIMO, the implementation of choice for active antennas was derived from military phased arrays. These classical phased arrays form true beams but suffer from extremely high costs even for limited surveillance applications. Their application to commercial wireless is further challenged by the complexity of industry use cases which require many simultaneous beams and maximum uplink and downlink transmission speeds over many users. Nevertheless, true beamforming is necessary in commercial mm-wave systems to be able to reach users given the large path loss at these frequencies.

After reviewing the history and attributes of existing Ma-MIMO and phased array systems, a new Ma-MIMO solution will be outlined which starts by addressing a fundamental limitation that both existing systems have: the overhead and inaccuracies involved in either directly attempting to achieve RF coherency across the array or some digitally produced substitute. Combining an analog IC innovation – first described in a 2006 CICC poster as applied to VLSI clock skew alignment – with additional radio architecture innovations, a hybrid Ma-MIMO system has been developed which builds MIMO processing on top of a fully synchronized array. Very well-defined beam shapes can then be produced for both TDD and FDD bands at much lower hardware complexity. Performance gains have been demonstrated in multiple live carrier trials, including clustered sectors which is a first for any Ma-MIMO system.

Session 2 - Wireline Techniques for Advanced Modulation Schemes

Monday, April 9, 10:00 am, Great Room 1-3

Session Chair: Eric Naviasky, Cadence

Session Co-Chair: Tzu-Chien Hsueh, Intel

This session showcases wireline techniques utilizing advanced modulation for proximity, body area networks, backplane, and optical data communication. The papers include an invited paper on contactless data links, ADC-DSP and mixed signal PAM-4 SERDES and an Optical front end.

10:00 am **Introduction**

2-1
10:05 am **High-Speed Contactless I/O for Computing Devices (Invited)**, C. Thakkar, J. Jaussi, B. Casper, Intel Corporation

Enabling content-rich consumer devices in a portable form-factor is enhanced by contactless I/O to support distributed computing and peripherals. Within such a personal computing space (1mm-1m), high-speed solutions (>10Gb/s) may be achieved with either near-field coupling-based proximity communication or far-field mm-wave wireless communication. In order to optimize proximity link performance based on data-rate, communication distance, coupler footprint and scalability to multi-channel I/O, this work develops analytical models of the contactless channel. The paper also highlights the tradeoffs between energy-efficiency and achievable communication distance in proximity and mm-wave wireless I/Os, along with two illustrative link designs at 32Gb/s and 27.8Gb/s respectively.

2-2
10:55 am **A Process and Temperature Insensitive CMOS Linear TIA for 100 Gbps/ λ PAM-4 Optical Links**, Kadaba Lakshmikummar, Alexander Kurylak, Manohar Nagaraju, Richard Booth, Joe Pampanin, Cisco Systems

A PVT insensitive linear TIA for 53 GBd PAM-4 optical links is reported. The 16nm FinFET CMOS chip consumes 61 mW with < 2 % THD at 600 mVpp differential swing, 27 GHz bandwidth, input referred noise density 18.3 pA/ $\sqrt{\text{Hz}}$, and transimpedance range of 63 to 80 dB Ω .

2-3
11:20 am **A 32 Gb/s ADC-Based PAM-4 Receiver with 2-bit/Stage SAR ADC and Partially-Unrolled DFE, (*Outstanding Student Paper Nominee*)**, S. Kiran, S. Cai, Y. Luo, S. Hoyos, S. Palermo, Texas A&M University

A PAM-4 ADC-based receiver employs a 32-way time-interleaved 6-bit 2-bit/stage loop-unrolled SAR ADC with a single capacitive reference DAC. Digital equalization complexity is reduced with a new PAM-4 DFE architecture that has a gate count comparable to an NRZ DFE, while simultaneously halving the critical path delay. A 3-tap FFE is embedded in the ADC using an additional non-binary DAC to improve the coverage of the 6-bit FFE coefficient space. This 3-tap embedded FFE and CTLE front-end partial equalization allows placement of the CDR's Mueller-Muller phase detector directly at the ADC output to avoid excessive loop delay. Fabricated in GP 65nm CMOS, the 32Gb/s receiver operates at a BER < 10⁻¹¹ with a 27 dB loss channel and < 10⁻⁹ with a 30 dB loss channel without utilizing any transmit equalization. The complete ADC-based receiver achieves a power efficiency of 8.25pJ/bit, including all the front-end, ADC, and DSP power.

2-4
11:45 am **A 56 Gb/s PAM4 Receiver with Low-Overhead Threshold and Edge-Based DFE FIR and IIR-Tap Adaptation in 65nm CMOS, (*Outstanding Student Paper Nominee*)**, A. Roshan-Zamir, T. Iwai, Y.-H. Fan, A. Kumar, H. W. Yang, L. Sledjeski*, J. Hamilton*, S. Chandramouli*, A. Aude*, S. Palermo, Texas A&M University, *Texas Instruments Corporation

A PAM4 quarter-rate receiver employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-taps to efficiently compensate for channel loss. In addition to the per-slice main 3 data samplers, an error sampler is utilized for background threshold control and an edge-based sampler performs both PLL-based CDR phase detection and generates information for background DFE tap adaptation. Fabricated in GP 65nm CMOS, the 56Gb/s receiver achieves 4.63mW/Gb/s and compensates for up to 20.8dB loss when operated with a 2-tap FFE transmitter.

Session 3 - Forum-Self Driving Car Technology and Associated Computational Power Requirements

Monday, April 9, 10:00 am, Great Room 4 Room

Forum Chairs: Charles Augustine, Intel, and A. Raychowdhury, Georgia Tech

- 10:00 am **Introduction**
- 3-1
10:05 am **Self-Driving Car Technology and Associated Computational Power Requirements**, Manoj Kaul, Texas Instruments
- 3-2
0:35 am **Computation Challenges for Artificial Intelligence Closer to the User**, Omesh Tickoo, Intel Corporation
- 3-3
11:05 am **Self-driving Cars and Lidar**, Simon Verghese, Waymo
- 3-4
11:35 am **Human Centered Autonomous Driving**, Mohan Trivedi, UC San Diego

Session 4 - Advanced RF Transceivers

Monday, April 9, 10:00 am, Great Room 5

Session Chair: Yanjie Wang, Intel

Session Co-Chair: Debopriyo Chowdhury, Broadcomm

State-of-the-art wireless systems implemented in CMOS process are presented. The session begins with advanced full-duplex circuits and systems, followed by a reconfigurable digital transmitter and finally ends with a high-performance RF receiver front end.

- 10:00 am **Introduction**
- 4-1
10:05 am **Integrated CMOS Transceivers Design Towards Flexible Full Duplex (FD) and Frequency Division Duplex (FDD) Systems (Invited)**, K. Chu, M. Katanbaf, C. Su, T. Zhang*, J. C. Rudell, University of Washington, *Verily Life Sciences
- This paper provides an overview of both the challenges and current state-of-the-art in the areas of full-duplex and frequency-division duplex integrated transceivers. Some recent single-chip full-duplex radios implemented in 40nm CMOS are highlighted, that range in low-power cancellation techniques, to transceivers which target >40MHz bandwidth using high power transmitters.
- 4-2
10:55 am **A Full-Duplex Transceiver Front-End RFIC with Code-Domain Spread Spectrum Modulation For Tx Self-Interference Cancellation and In-Band Jammer Rejection, (*Outstanding Regular Paper Nominee*)**, Zhen Qi Chen, Dongyi Liao, Fa Foster Dai, Auburn University
- This paper presents a code-domain spread spectrum modulation scheme for full-duplex transceiver front-end with dual function of in-band jammer rejection and transmitter self-interference cancellation. The front-end achieves 18.8dB in-band jammer rejection and up to 51dB Tx self-interference suppression.
- 4-3
11:20 am **A Compact 2.4GHz Polar/Quadrature Reconfigurable Digital Power Amplifier in 28nm Logic LP CMOS, (*Outstanding Student Paper Nominee*)**, Y. Zhu, L. Xiong, Y. Yin, W. Luo, B. Chen, T. Li, H. Xu, Fudan University

This paper presents a compact dual-mode reconfigurable transformer-combined digital PA that supports polar and quadrature transmitters. Both modes employ the load modulation to enhance backoff efficiency, and an efficiency peaking at 6dB PBO is achieved in polar mode. Both modes achieve competitive performance in terms of resolution, linearity and efficiency.

4-4
11:45 am **A Low-Power Sub-GHz RF Receiver Front-end with Enhanced Blocker Tolerance**, Z.Jiang, D.Johns, A.Liscidini, University of Toronto

This paper presents a sub-GHz RF receiver front-end suitable for ultra-low power application. The class-AB operation in both the RF and baseband sections leads to a very low sensitivity and an elevated blocker tolerance. Such performance makes the receiver suitable for both short-range (e.g. 802.15.4) and long-range (e.g. LoRa) applications.

Session 5 - Advanced Analog Techniques

Monday, April 9, 10:00 am, Great Room 6-8

Session Chair: Ivan O'Connell, University College Cork

Session Co-Chair: Hiroki Ishikuro, Keio University

This session will present analog techniques ranging from high voltage drivers to reference generation, including an invited paper on noise filtering.

10:00 am **Introduction**

5-1
10:05 am **180Vpp Output Voltage, 24MHz Bandwidth, Low Power Class AB Current-Feedback High Voltage Amplifier for Ultrasound Transmitters**, D. Ghisu, A. Gambero, M. Terenzi, G. Ricotti, A. Moroni, S. Rossi, STMicroelectronics

A novel integrated high-voltage high-bandwidth linear amplifier for medical ultrasonic applications is presented. It's capable of transmitting a 180Vpp sine wave signal up to 20MHz with a second-order harmonic distortion lower than -43dB, a slew-rate of 12V/ns and dissipating only 20mW with a 0.1% duty-cycle, while driving a 300pF||100Ω load.

5-2
10:30 am **System-Level Noise Filtering and Linearization (Invited)**, T. He, G. C. Temes, Oregon State University

The performance of analog integrated circuits is often limited by the noise generated in its components. Several circuit techniques exist for suppressing the effects of the low-frequency noise. In this paper, existing techniques are described for noise mitigation. Also, a novel approach is proposed, which can suppress low-frequency noise.

5-3
11:20 am **A Diode-Less Compact Voltage/Frequency Reference-in-One**, Alfio Zanchi, The Boeing Company

A circuit class of voltage references is introduced, substituting diodes in a Widlar cell with non-linear switched-capacitor resistors realized with VCOs (f-VR) or varactors (c-VR). Autonomous f-VRs provide a voltage/frequency reference-in-one (1.24V/30.4MHz). 90nm-CMOS prototypes exhibit 7ppm/°C voltage, 15ppm/°C frequency TC across -40/+120°C. These diode-less circuits can tolerate 300Krad(Si) radiation dose.

Session 6 - Power Management Circuits and Architectures

Monday, April 9, 1:30 pm, Great Room 1-3

Session Chair: Hanh-Phuc Le, University of Colorado, Boulder

Session Co-Chair: Tufan Karalar, Istanbul TU

Power management circuits and architectures, including digital-controlled LDO, advanced mode transitions stacked voltage domain, multiple outputs, wireless power transfer, switched-capacitor, multi-level, hybrid and fully-integrated DC-DC converters.

1:30 pm **Introduction**

6-1
1:35 pm **Pathways to mm-Scale DC-DC Converters: Trends, Opportunities, and Limitations (Invited)**, Jason T. Stauth, Dartmouth College

6-2
2:25 pm **A Capacitive DC-DC Converter for Stacked Loads With Wide Range DVS Achieving 98.2% Peak Efficiency in 40nm CMOS**, T. Thielemans, N. Butzen, A. Sarafianos, M. Steyaert, F. Tavernier, ESAT-MICAS KULeuven

A combination of Voltage Domain Stacking and Dynamic Voltage Scaling offers significant efficiency improvements in both the power delivery and the functional blocks. This paper presents a fully integrated gearbox-type switched capacitor DC-DC converter with a threefold control loop, achieving the widest DVS-range for stacked independent loads.

6-3
2:50 pm **A 78%-Efficiency Li-ion-Compatible Fully-Integrated Modified 4-Level Converter with 0.01-40mW DCM-Operation in 28nm FDSOI**, Sally Safwat Amin, Patrick P. Mercier, University of California, San Diego

This paper presents a battery-connected DC-DC converter integrated in a scaled CMOS process. To achieve high efficiency while blocking the 2.8-4.2V Li-ion battery voltage range using only 1.5V transistors, a modified 4-level buck converter is proposed. Implemented in 28nm FDSOI, the converter switches at up to 200MHz, regulating down to 0.6-1.0V over a 10uW-40mW output power range via use of DCM-PFM control. The converter occupies 1.5mm² of silicon area (including includes a pair of 5nF flying capacitors and a 3nH inductor), and achieves a peak efficiency of 78%

3:15 PM **BREAK**

6-4
3:30 pm **An AC-Coupled Stacked Dual Active Bridge Hybrid DC-DC Converter for Battery-to-Processor Power Delivery with 87.2% Peak Efficiency and High Accuracy Loadline Regulation**, Yongjun Li, Mervin John*, Yogesh Ramadass*, Seth R. Sanders, University of California, Berkeley, *Texas Instrument

This works presents a hybrid 3:1 DC-DC converter topology with the use of standard CMOS switches and utilizing the loop of package interconnection in sub 10nH range as effective inductor. The prototype achieves power density of 0.46W/mm² with 83.4% efficiency and 50mV output perturbation under a 0.4A load step

6-5
3:55 pm **A Switching Linear Regulator Based on a Fast-Self-Clocked Comparator with Very Low Probability of Meta-Stability and a Parallel Analog Ripple Control Module**, S. Kudva, S. Song, J. Poulton, J. Wilson, W. Zhao*, C. Gray, Nvidia Corporation, *North Carolina State University

POL regulators are critical in low power systems. A linear regulator with a comparator that samples the error at 4GHz using a novel self-clocking scheme to achieve extremely low probability of metastability is presented. Zero droop for load current step of 170mA/100ps and peak current efficiency of 97.6% is achieved.

6-6
4:20 pm **Self-Regulated Voltage/Current-Mode Integrated Power Management with Seamless Mode Transition and Extended Input-Voltage Range**, Hesam Sadeghi Gougheri, Mehdi Kiani, Pennsylvania State University

An integrated power management (IPM) structure for inductive power delivery is presented with the capabilities of seamless transition between voltage and current mode operations, extended input-voltage range, self-regulation, and over-voltage protection with only one off-chip capacitor.

6-7
4:45 pm **Single-Stage Dual-Output AC-DC Converter for Wireless Power Transmission**, Zhongming Xue, Shiquan Fan, Lina Zhang, Zhuoqi Guo, Li Dong, Dan Li, Li Geng, Xi'an Jiaotong University

Wireless power transmission (WPT) system is widely used in implantable biomedical applications. Conventional power management unit (PMU) in the secondary side normally consists of rectifier and DC-DC converters in series, which shows low power conversion efficiency (PCE). In this work, we propose a single-stage AC-DC converter with dual regulated-outputs, combining output regulation with full-wave active rectifier, which not only improves the power efficiency, but also saves silicon area.

6-8
5:10 pm **Switched Inductor Capacitor Buck Converter with >85% Power Efficiency in 100 μ A-to-300mA Loads using a Bang-Bang Zero-Current Detector**, Jongbeom Baek^{1,2}, Ji-Hun Lee¹, Se-Un Shin¹, Min-young Jung² and Gyu-Hyeong Cho¹, ¹Korea Advanced Institute of Science and Technology (KAIST), ²Samsung Electronics

In this paper, an accurate bang-bang zero-current detector to prevent reverse inductor current and a triple mode switched inductor-capacitor buck converter to extend load range are presented. The proposed converter sustains minimum power conversion efficiency of 85% in the output load range from 100uA to 300mA.

Session 7 - Sensor Interface Techniques

Monday, April 9, 1:30 pm, Great Room 4

Session Chair: Nagendra Krishnapura, IIT Madras

Session Co-Chair: Maysam Ghovanloo, Georgia Institute of Technology

In this session we have papers describing circuits for sensing biosignals, current, sound, and temperature, as well as an invited paper reviewing energy-efficient bridge-to-digital converters.

1:30 pm **Introduction**

7-1
1:35 pm **A 0.6V 3.8 μ W ECG/Bio-Impedance Monitoring IC for Disposable Health Patch in 40nm CMOS**, J. Xu*, Q. Lin**, M. Ding*, Y. Li**, C. Van Hoof*, W. Serdijn**, N. Van Helleputte*, *Imec, **Delft University

This work presents a 0.6V 3.8 μ W analog front-end IC for simultaneous recording of ECG and bio-impedance. The IC can measure both signals simultaneously with the same electrodes and one single IA, it advances prior-art ICs with at least 2x lower supply voltage and 15x lower power.

7-2
2:00 pm **Design of a 3.24 μ W, 39nV/ \sqrt Hz Chopper Amplifier With 5.5Hz Noise Corner Frequency for Invasive Neural Signal Acquisition**, Deng Luo, Milin Zhang, Zhihua Wang, Tsinghua University

This paper proposes a low noise, low power and low THD amplifier with chopper modulation topology for biosignal acquisition. A Gm-C integrator based DC-servo-loop

with complementary input scheme is proposed to achieve high linearity while maintaining low noise. A THD of -61dB and thermal noise PSD of $39\text{nV}/\sqrt{\text{Hz}}$ are achieved.

7-3
2:25 pm **Energy-Efficient Bridge-to-Digital Converters (Invited), (*Outstanding Invited Paper Nominee*)**, H. Jiang and K. A. A. Makinwa, Delft University of Technology

This paper presents an overview of energy-efficient systems intended for the digital readout of Wheatstone bridge sensors. Apart from energy-efficiency, such bridge-to-digital converters (BDCs) must achieve low input-referred offset, drift and noise; high gain accuracy, stability and linearity; as well as high immunity to power-supply and common-mode variations. Various BDC architectures will be discussed, beginning with classical ones in which an instrumentation amplifier is followed by an analog-to-digital converter (ADC), and moving on to more recent ones, which attempt to reduce complexity by eliminating the instrumentation amplifier and connecting an ADC directly to a bridge. The performance of these topologies, and in particular their energy-efficiency, will be compared and summarized.

3:15 PM **BREAK**

7-4
3:30 pm **A Fully Integrated DC to 75MHz Current Sensing Circuit with On-Chip Rogowski Coil**, Tobias Funk, Bernhard Wicht*, Robert Bosch Center for Power Electronic of Reutlingen University, *Leibniz University Hannover

A wide-bandwidth galvanically isolated current sensing circuit with integrated Rogowski coil is presented. Based on the Rogowski coil's high-frequency properties, currents can be measured up to 75MHz. The sensor front-end comprises two integrators, which allows chopper frequencies below signal bandwidth. An integrated Hall sensor extends the measurement range towards DC.

7-5
3:55 pm **Pseudo-Differential Analog Readout Circuit for MEMS Microphones performing 135dB SPL AOP and 66dBA SNR at 1Pa**, F. Barbieri, A. Barbieri, G. Nicollini, STMicroelectronics

An Analog Readout Circuit for Capacitive MEMS microphones is presented. Thanks to an innovative architecture, it combines the advantages in terms of robustness, cheapness, and industrialization of Single-Backplate MEMS Microphones with input dynamic range and rejection to spurs proper of Dual-Backplate solutions.

7-6
4:20 pm **A 13nW Temperature-to-Digital Converter Utilizing Sub-threshold MOSFET Operation at Sub-thermal Drain Voltage, (*Outstanding Student Paper Nominee*)**, T. Someya, A.K.M.M. Islam, T. Sakurai, M. Takamiya, University of Tokyo

The proposed external-reference-free temperature-to-digital converter with on-chip PTAT digital output based on the sub-threshold current in deep triode region achieved the lowest power consumption of 13nW at 0.8V supply with 110mK resolution and $-0.7/+1.3^\circ\text{C}$ inaccuracy over a temperature range of $-20-80^\circ\text{C}$.

Session 8 - Human Body Communications and Emerging Applications

Monday, April 9, 1:30 pm, Great Room 5

Session Chair: Kaushik Sengupta, Princeton University

Session Co-Chair: Marco Tartagni, University of Bologna

This session will explore emerging technologies for application in human body and will survey new materials and devices for sensing.

1:30 pm

Introduction

8-1
1:35 pm

Artificial Intelligence Meets Large-Scale Sensing: using Large-Area Electronics (LAE) to enable intelligent spaces (Invited), M. Ozatay, L. Aygun, H. Jia, P. Kumar, Y. Mehlman, C. Wu, S. Wagner, J. C. Sturm, N. Verma, Princeton University

Large-Area Electronics enables unobtrusive deployment of sensors on a large number of objects. This paper explores the potential this raises to efficiently learn models for state estimation and action planning in smart spaces, by exploiting the correspondence between our natural interactions with physical objects, and our underlying activities and intentions.

8-2
2:25 pm

Highly-Integrated Guidewire Vascular Ultrasound Imaging System-on-a-Chip, J. Lim, C. Tekes*, A. Rezvanitabar, E. F. Arkan*, F. L. Degertekin*, M. Ghovanloo, ECE-Georgia Tech, *ME-Georgia Tech

To produce real-time images for the cardio-vascular interventions, in this study, we present a highly integrated guidewire ultrasound imaging system-on-a-chip (GUISoC) implemented in 0.18- μm high voltage (HV) CMOS process which requires three wires for the interconnection. The system generates high voltage pulses exciting a capacitive micromachined ultrasound transducer (CMUT) array in transmit mode and captures echo signals scattered from the imaging medium in receive mode. Quadrature sampler down-converts 25-38 MHz echo signals from 12-elements CMUT array to baseband, and I/Q signals are multiplexed through a 2-m long 52-AWG coaxial cable. The 3 mm² GUISoC is powered and clocked through three wires, while consuming 25.2 mW and 46 mW at 1.8 V and 46 V supplies, respectively.

8-3
2:50 pm

A 6.3pJ/b 30Mbps -30dB SIR-tolerant Broadband Interference-Robust Human Body Communication Transceiver using Time Domain Signal-Interference Separation, Shovan Maity, Baibhab Chatterjee, Gregory Chang, Shreyas Sen, Purdue University

This paper presents a broadband HBC transceiver implemented in 65nm CMOS that achieves 6.3pJ/b, 30Mbps, -30dB interference-tolerant operation. Time Domain Signal-Interference Separation (TD-SIS) using Integrating DDR (I-DDR) receiver allows tolerance to -30 dB SIR with BER <10⁻³. This transceiver achieves 18X improvement in energy-efficiency compared to the State-of-the-Art HBC transceivers.

3:15 PM

BREAK

8-4
3:30 pm

A CMOS Inductorless MedRadio OOK Transceiver With a 42 μW Event-Driven Supply-Modulated RX and a 14% Efficiency TX for Medical Implants, Mao-Cheng Lee, Alireza Karimi-Bidhendi, Omid Malekzadeh-Arasteh, Po T. Wang*, Zoran Nenadic*, An H. Do**, Payam Heydari, Department of Electrical Engineering and Computer Science, University of California, Irvine, *Department of Biomedical Engineering, University of California, Irvine, **Department of Neurology, University of California, Irvine

An inductorless OOK TRX for medical implants in 180nm CMOS is presented. An event-driven supply modulation technique is introduced in RX to lower the power consumption to 42/92 μW at 1/10kbps, achieving -79/-74dBm sensitivity. The transmitter employs a current-starved oscillator with a frequency calibration loop, achieving 14% efficiency at -4dBm Pout.

8-5
3:55 pm

A Receiver/Antenna Co-Design for a 1.5mJ per Fix Fully-Integrated 10x10x6mm³ GPS Logger, Hyeongseok Kim, Nikolaos Chiotellis, Elnaz Ansari, *Muhammad Faisal, Taekwang Jang, Anthony Grbic, Hun-Seok Kim, David Blaauw, David Wentzloff, University of Michigan, *Movellus

An ultra-low power GPS logger features miniaturized antenna co-designed with GPS AFE optimized for heavy duty-cycling and $10 \times 10 \times 6 \text{mm}^3$. It achieves 10dB SNR at -125dBm. While 1.5mJ energy per fix, the logger store data for 37 position fixes over 10ms of received signal per fix to flash for later egress and post-processing.

8-6
4:20 pm **Adiabatically Driven Touch Controller Analog Front-End for Ultra-thin Displays**, Jiheon Park, Young-Ha Hwang, Jonghyun Oh, Jun-Eun Park, , Deog-Kyoon Jeong, Dept. of electrical and computer engineering, Seoul National University

To overcome adverse effects of recent incorporated touch-display panel development, this paper presents an analog front-end (AFE) of a touch controller with the adiabatic stimuli generation and noise-sampling-embedded modulation. The AFE provides a 51.5dB SNR at 120Hz frame rate and achieves a 14.7dB SNR improvement via the noise sampling.

8-7
4:45 pm **Dual-mode, In-Pixel Linear and Single-Photon Avalanche Diode Readout for Low-Light Dynamic Range Extension in Photodetector Arrays**, H. Ouh, M.L. Johnston, Oregon State University

Linear and single-photon avalanche photodiode operation are combined in a single pixel to enhance low-light dynamic range. An 8×8 array fabricated in 180nm CMOS demonstrates 85dB optical dynamic range and 130Hz maximum frame-rate. This represents the first reported photodetector array architecture supporting both linear and single-photon operation within each pixel.

8-8
5:10 pm **A Programmable CMOS Transceiver for Structural Health Monitoring**, Xinyao Tang, Haixiang Zhao, Soumyajit Mandal, Case Western Reserve University

We describe a highly-integrated CMOS transceiver for active structural health monitoring (SHM). The chip actuates piezoelectric transducers and also senses ultrasound waves received by the same or another transducer. The transmitter uses an integer-N frequency synthesizer and pulse-width modulation (PWM) to generate low-distortion, band-limited waveforms up to $12.7 V_{pp}$ with center frequency from ~ 0.1 -2.75 MHz. The integrated offset-canceling fully-differential receiver has programmable gain and bandwidth, and uses quadrature demodulation to extract both amplitude and phase of the received waveforms for further signal processing. The transceiver was fabricated in a $0.5\mu\text{m}$ CMOS process and has been validated using (2D) damage localization on an SHM test bed.

Session 9 - High Performance Oscillators and Low-Power Digital Clock Generation

Monday, April 9, 1:30 pm, Great Room 6-8

Session Chair: Amr Fahim, Inphi

Session Co-Chair: Woogeun Rhee, Tsinghua University

This session presents high-performance VCOs and low-power digital clock generation building blocks. This session begins with two high-performance VCOs demonstrating state-of-the-art noise circulation techniques and novel quadrature VCO design. The third paper presents a fully synthesizable digital PLL. The final paper describes a low jitter wide-dynamic range DTC.

1:30 pm **Introduction**

9-1
1:35 pm **A Noise Circulating Cross-Coupled VCO with a 195.6dBc/Hz FoM and 50kHz 1/f³ Noise Corner, (*Outstanding Student Paper Nominee*)**, F. Wang, H. Wang, Georgia Institute of Technology

This paper presents a noise circulating VCO topology that suppresses both the 1/f² and 1/f³ phase noise over a wide tuning range. A prototype VCO at 2.35GHz is implemented in a 130nm CMOS process. The measured FoM is 195.6 dBc/Hz at 10MHz offset with a 50kHz 1/f³ phase noise corner.

9-2
2:00 pm **Low Noise RF Quadrature VCO Using Tail-Switch Network-Based Coupling in 40 nm CMOS**, Venkatraman Natarajan, Mohammadhossein Naderi Alizadeh, Jose Silva-Martinez, Texas A&M University

The proposed VCO presents an alternative approach to obtaining accurate quadrature phases by strategically modulating tail current sources while avoiding bimodal oscillations and noise due to coupling paths; the architecture is very compact, low power, robust and does not require tuning knobs. Demonstrated in a 40 nm CMOS process, the measured phase noise is -123.2 dBc/Hz at 1 MHz offset for an oscillation frequency of 4.9 GHz. The measured phase error at 4.9 GHz is 1.4°. A figure of merit (FoM) of 188.3 dBc/Hz was obtained while dissipating a power of 7.5 mW from a 1.1 V power supply.

9-3
2:35 pm **A 1.2ps-Jitter Fully-Synthesizable Fully-Calibrated Fractional-N Injection-Locked PLL Using True Arbitrary Nonlinearity Calibration Technique**, Bangan Liu, Huy Cu Ngo, Kengo Nakata, Wei Deng, Yuncheng Zhang, Junjun Qiu, Toru Yoshioka, Jun Emmei, Haosheng Zhang, Jian Pang, Aravind Tharayil Narayanan, Dongsheng Yang, Hanli Liu, Kenichi Okada and Akira Matsuzawa, Tokyo Institute of Technology

This paper presents a fully-synthesizable Fractional-N injection-locked PLL with extensive digital calibration in 65nm CMOS. The RMS jitter of 1.2ps and 0.3ps is achieved at 1GHz output for Fractional-N and Integer-N operation, respectively. The power consumption is 2.5mW and 2.2mW, corresponding to an FoM of -234.4dB and -246.7dB.

9-4
2:50 pm **A 1.6ps peak-INL 5.3ns range two-step digital-to-time converter in 65nm CMOS**, Ahmed Elmallah, Mostafa Gamal Ahmed, Ahmed Elkholy, Woo-Seok Choi, Pavan Kumar Hanumolu, University of Illinois at Urbana-Champaign

A wide range high resolution 2-stage digital-to-time converter (DTC) is presented. It uses a counter in the first stage and a digitally controlled delay line in the second stage to decouple the range versus resolution trade-off. Background calibration is used to correct interstage gain error. Fabricated in 65nm, the prototype DTC achieves 1:65ps-peak-integral non-linearity (INL) while consuming 10:13mW at 100MHz carrier frequency. The achieved dynamic range is 15dB higher than state-of-the-art DTCs.

3:15 PM **BREAK**

Session 10 - Forum- The Next Waves of Machine and Deep Learning Hardware:

Monday, April 9, 3:30 pm, Great Room 5-8

Forum Chairs: Jae-sun Seo, ASU, and Mingoo Seok, Columbia University

3:30 pm **Introduction**

10-1
3:35 pm **Design Considerations for Deep Learning Hardware Acceleration**, Leland Chang, IBM

10-2
4:05 pm **Understanding the Limitations of Existing Energy-Efficient Design Approaches for Deep Neural Networks**, Vivienne Sze, MIT:

- 10-3
4:35 pm **Training Deep Neural Networks on a Reconfigurable Non-Von Neumann Computer Architecture**, Chris Nicol, Wave Computing
- 10-4
5:05 pm **Narrowing the Computational Efficiency Gap Between Artificial and Natural Intelligence**, Anand Raghunathan, Purdue
- 10-5
5:35 pm **Mixed-Signal Nanoelectronic Neurocomputing**, Dmitri Strukov, UCSB

Session 11 - CMOS Biochips and Bioelectronics

Tuesday, April 10, 8:30 am, Great Room 1-3

Session Chair: Rikky Muller, University of California, Berkeley

Session Co-Chair: Jerald Yoo, National University of Singapore

This session presents an overview of the challenges, opportunities and latest advances in CMOS biochips and bioelectronics. Topics include invitro diagnostics, implantable sensors, and miniaturized neural interfaces.

8:30 am **Introduction**

11-1
8:35 am **CMOS Biochips: Challenges and Opportunities (Invited), (*Outstanding Invited Paper Nominee*)**, A. Hassibi, N. Wood, A. Manickam, InSilixa, Inc.

CMOS-integrated biosensors, generally referred to as CMOS biochips and their underlying technologies are discussed in this paper. These devices are used in biotechnology to precisely detect and study bio-molecular analytes from biological samples in a massively parallel fashion. While CMOS biochips offer cost-efficiency, scalability, ease-of-use, and robustness for biosensing applications, their growth and adoption has been limited in the past two decades. The rationale behind this shortcoming is discussed in this paper and possible solutions are presented.

11-2
9:25 am **A 16x20 Electrochemical CMOS Biosensor Array with In-Pixel Averaging Using Polar Modulation**, Chung-Lun Hsu*, Alexander Sun*, Yunting Zhao*, Eliah Aronoff-Spencer**, Drew A. Hall*, *Department of Electrical and Computer Engineering University of California San Diego, ** School of Medicine University of California San Diego

We report a 16x20 electrochemical biosensor array with on-chip sensors that implements a polar-mode measurement allowing the readout circuitry to be mostly digital and small. Implemented in a 0.18 μm process, the 3x4 mm² chip achieves state-of-the-art with an rms phase error of 0.04% at 50 kHz and measured hybridization of Zika virus oligonucleotides.

11-3
9:50 am **A Sub-1 μW Multiparameter Injectable BioMote for Continuous Alcohol Monitoring, (*Outstanding Student Paper Nominee*)**, H. Jiang, X. Zhou, S. Kulkarni, M. Uranian, R. Seenivasan, D. Hall, University of California San Diego

This paper presents an injectable, fully-integrated, 0.85x1.5mm² sensor chip for continuous, long-term alcohol monitoring consuming 970nW. It harvests power wirelessly and transmits data through backscatter. A micro-electrochemical sensor array measures ethanol differentially to remove interference. A low-power potentiostat supports both amperometric and potentiometric techniques achieving 2.5nA and 0.5mV sensitivity, respectively.

10:15 AM **BREAK**

11-4
10:40 am **CMOS electronics probe inside a cellular network (Invited)**, Jeffrey Abbott, Ling Qin, Tianyang Ye, Marsela Jorgolli, Rona S. Gertner, Hongkun Park, Donhee Ham, Harvard University

Parallelization of intracellular recording can greatly benefit neuroscience and cardiology, but it has been difficult. Our recent large-scale array of vertical nanoelectrodes on a CMOS integrated circuit hit a milestone by recording from 235 networked cardiomyocytes in parallel. This paper reviews this work, focusing especially on the CMOS integrated circuit.

11-5
11:05 am **StimDust: A 6.5mm³, Wireless Ultrasonic Peripheral Nerve Stimulator with 82% Peak Chip Efficiency, (*Outstanding Regular Paper Nominee*)**, Benjamin C. Johnson, Konlin Shen, David Piech, M. Meraj Ghanbari, Ka Yiu Li, Ryan Neely, Jose M. Carmena, Michel M. Maharbiz, Rikky Muller, University of California, Berkeley

We present a 6.5mm³, 10mg, wireless peripheral nerve stimulator with 82% stimulation efficiency and high temporal precision. The stimulator is powered and controlled through ultrasound from an external transducer and utilizes a single piezocrystal and IC. The encapsulated stimulator was cuffed to the sciatic nerve of an anesthetized rodent and demonstrated full-scale nerve activation.

11-6
11:30 am **Towards a 1.1 mm² Free-Floating Wireless Implantable Neural Recording SoC**, P. Yeon, M.S. Bakir, M. Ghovanloo, Georgia Institute of Technology

A 1.1 mm² sized free-floating wireless implantable neural recording (FF-WINeR) system-on-a-chip (SOC) is designed and tested in-vitro toward developing a stand-alone neural probe in the form of small untethered pushpins (1 mm³) to be distributed across the areas of interest in the brain.

11-7
11:55 am **A Wireless, Low-Drift, Implantable Intraocular Pressure Sensor with Parylene-on-oil Encapsulation**, A. Agarwal, A. Shapero, D. Rodger*, M. Humayun*, YC. Tai, A. Emami, California Institute of Technology, *USC Keck School of Medicine

A wireless, implantable continuous intraocular pressure monitor featuring parylene-on-oil sensor encapsulation for achieving long-term low-drift in vivo is presented. It achieves a pressure sensitivity of 0.17 mmHg with a total power consumption of 9.7μW. We demonstrate offset drift of <0.5 mmHg for over 4 months over temperatures of 27-38 °C.

Session 12 - Forum-The Vanishing Boundary between Digital and Analog

Tuesday, April 10, 8:30 am, Great Room 4

Forum Chairs: Shreyas Sen Purdue University, and A. Raychowdhury Georgia Institute of Technology

8:30 am **Introduction**

12-1
8:35 am **Digital Circuits with Analog Behavior**, Keith Bowman, Qualcomm

12-2
9:05 am **Digital-Friendly Transceivers**, Elad Alon, University of California, Berkeley

12-3
9:35 am **VLSA (Very Large-Scale Analog): Cell-Based, Synthesized ADPLLs**, David Wentzloff, University of Michigan

12-4
10:05 am **Digital Friendly LDOs: Opportunities and Control**, Harish Krishnamurthy, Intel Labs

10:35 am **BREAK**

Session 13 - THz, mmWave & RF Techniques

Tuesday, April 10, 8:30 am, Great Room 5

Session Chair: Swaminathan Sankaran, Texas Instruments

Session Co-Chair: Aritra Banerjee, IMEC, Florida

State-of-Art high frequency and wide bandwidth circuits and system techniques for communication concluding 5G, "wired", and sensing applications will be presented.

8:30 am **Introduction**

13-1
8:35 am **Circuit and Antenna-in-Package Innovations for Scaled mmWave 5G Phased Array Modules (Invited), (*Outstanding Invited Paper Nominee*)**, A. Valdes-Garcia, B. Sadhu, X. Gu, Y. Tousi, J. Haillin*, S. Sahl*, D. Liu, S. Reynolds, L. Rexberg*, IBM, *Ericsson

Directional communication at millimeter-wave (mmWave) frequencies is one of the key technologies under development towards the anticipated deployment of fifth generation mobile access (5G). Silicon-based multi-antenna systems are strong candidates for the implementation of such directional links, however, the performance requirements are in general significantly more challenging than those posed by mmWave WLAN links demonstrated so far (e.g. for 802.11ad). This work presents an overview of recent innovations in circuit design, antenna design, and beamforming architecture which enable complex phased arrays with precise and agile beamforming for mmWave-based 5G communications.

13-2
9:25 am **A 64-67GHz Partially-Overlapped Phase-Amplitude-Controlled 4-Element Beamforming-MIMO Receiver**, H. Mohammadnezhad, R. Abedi, A. Esmaili, P. Heydari, University of California, Irvine

A 4-element beamforming-MIMO receiver (RX) operating at 64-67GHz and capable of 2-stream reception is presented. By partially overlapping RX elements into two clusters of 3-element phased arrays, both beamforming's coherent processing gain and MIMO's multiplexing gain are achieved with reduced number of RF front-end resources.

13-3
9:50 am **A 26.6mW 1Gb/s Dual-Antenna Wideband Receiver with Auto Beam Steering for Secure Proximity Communications**, D. Liu, X. Huang, Z. Ding, H. Song, W. Rhee, Z. Wang, Tsinghua University

This paper describes a dual-path noncoherent receiver architecture with auto beam steering function. Two digital-assisted calibration loops are embedded in the bit slicer for robust high speed OOK demodulation. A prototype 6-8GHz dual-path receiver implemented in 65nm CMOS consumes 26.6mW at 1Gb/s with -54dBm sensitivity. The proposed receiver with high-resolution directivity not only mitigates the multipath fading effect but also adds security for smart mobile proximity communications.

10:15 AM **BREAK**

13-4
10:40 am **300-GHz CMOS QPSK Transmitter for 30-Gbps Dielectric Waveguide Communication, (*Outstanding Student Paper Nominee*)**, Q. Zhong, Z. Chen, N. Sharma, S. K. Shattri, W. Choi, K.K. O, The University of Texas at Dallas.

A 300-GHz 30-Gbps QPSK transmitter is demonstrated in 65-nm CMOS. The transmitter consists of an onchip multi-mode modulator, an injection locked quadrature oscillator, a

40-GHz bandwidth power amplifier with constant gain and group delay, a 4X frequency multiplier chain to generate a 165-GHz LO signal for a double balanced up-conversion mixer that generates the output at 300 GHz. The transmitter without equalization consumes 180mW with an energy efficiency of 6 pJ/bit

13-5
11:05 am **CMOS Terahertz Receivers (Invited)**, Q. Zhong¹, W.-Y. Choi¹, D.-Y. Kim², Z. Ahmad³, R. Xu⁴, Y. Zhang¹, R. Han⁵, S. Kshattri¹, N. Sharma⁶, Z.-Y. Chen¹, D. Shim⁷, S. Sankaran³, E.-Y. Seok³, C. Mao⁸, F. C. DeLucia⁹, J. P. McMillan⁹, C. F. Neese⁹, I. Kim¹⁰, I. Momson¹, P. Yelleswarapu¹, S. Dong¹, B. Pouya¹, P. Byreddy¹, Z. Chen¹, Y. Zhu¹, S. Ghosh¹, T. Dinh¹, F. Jalalibidgoli¹, J. Newman¹, K.K. O¹, ¹U. of Texas at Dallas, ²Qorvo, ³TI Inc., ⁴U. of Texas at Austin, ⁵MIT, ⁶Samsung Research America, ⁷SeoulTech, ⁸IDT, ⁹Ohio State U., ¹⁰UConn Health

Despite the fact that f_{max} of NMOS transistors has peaked around 320 GHz, it should be possible to coherently detect signals at frequencies beyond 1 THz and with some straightforward modification of processes, to incoherently detect signals at 40 THz in CMOS.

Session 14 - Nyquist ADC

Tuesday, April 10, 8:30 am, Great Room 6-8

Session Chair: Mike Chen, University of Southern California

Session Co-Chair: John Khoury, Silicon Laboratories

This session presents an overview of emerging ADC techniques. Several high-speed Nyquist ADCs with interleaved SARs. A pipelined ring-amplifier ADC and low-power design techniques.

8:30 am **Introduction**

14-1
8:35 am **Emerging Data Converter Architectures and Techniques (Invited)**, Gabriele Manganaro, Analog Devices Inc.

Emerging data converter architectures and techniques are here surveyed. Different drivers to technology innovation lead to a wide variety of implementations and capabilities. This paper aims to provide broad, though by no means exhaustive, snapshot of some interesting developments in this field.

14-2
9:25 am **A 1Gsps, 12-bit, Single-channel Pipelined ADC with Dead-zone-degenerated Ring Amplifiers, (*Outstanding Student Paper Nominee*)**, J. Lagos^{**}, B. Hershberg^{*}, E. Martens^{*}, P. Wambacq^{*}, J. Craninckx^{*}, imec, ^{**}Vrije Universiteit Brussel

Leveraging deadzone-degeneration and 2nd-stage bias enhancement techniques, a 12-bit, 1Gsps, single-channel ringamp-based ADC in 28nm CMOS achieves 56.6dB SNDR and 73.1dB SFDR consuming 24.8mW from a 0.9V supply, resulting in Schreier and Walden FoMs of 159.6dB and 45fJ/conv.-step.

14-3
9:50 am **A 31.5-GHz BW 6.4-b ENOB 56-GS/s ADC in 28nm CMOS for 224-Gb/s DP-16QAM Coherent Receivers**, K.Sun, G. Wang, P. Gui, Q. Zhang^{*}, S. Elahmadi^{*}, Southern Methodist University, ^{*}Menara Networks

This paper presents a 56GS/s 64-way time-interleaved ADC in 28nm CMOS. The ADC can meet the ENOB, BW and sampling rate requirements of a 224Gb/s DP-16QAM coherent receiver and is suitable for working as a 56Gb/s PAM-4 analog front-end in optical application. We propose a parametric track-and-hold amplifier and a switched sub-channel buffer to improve the SNR and linearity. The ADC achieves 6.4b ENOB at DC and greater than 5.2b ENOB up to the Nyquist frequency. The prototype utilizes multiple

bandwidth enhancing techniques and a hierarchical sampling architecture to enable the 31.5GHz BW and 56GS/s sampling rate, respectively. The power consumption of the entire ADC is 702mW.

10:15 AM **BREAK**

14-4
10:40 am **A 10-b 600-MS/s 2-Way Time-Interleaved SAR ADC with Mean Absolute Deviation Based Background Timing-Skew Calibration**, Jeonggoo Song, University of Texas at Austin, Nan Sun, University of Texas at Austin

This paper presents a time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with a novel mean absolute deviation (MAD) based timing-skew calibration technique. It features two highlights. First, Its computation complexity is very low, only involving subtraction and taking absolute value. Second, its convergence speed is fast with even random signals. A prototype 10-b 600-MS/s 2-way TI-SAR ADC in 40-nm CMOS achieves the peak SNDR of 56dB and 52 dB across the entire Nyquist band. Power consumption is 4.7mW and it leads to the Walden FoM of 23.8-fJ/conversion step.

14-5
11:05 am **A 0.0013mm² 10b 10MS/s SAR ADC with a 0.0048mm² 42dB-Rejection Passive FIR Filter, (*Outstanding Regular Paper Nominee*)**, P. Harpe, Eindhoven University of Technology

This work presents a small-size 10b 10MS/s SAR ADC with an integrated filter, consuming 39.2uW in 65nm CMOS. A new DAC layout technique results in an ADC area of 36x36um while achieving 9.18b ENOB. A 4x time-interleaved 15-tap passive FIR filter achieves >42dB rejection while occupying 53x90um.

CICC KEYNOTE LUNCHEON

Tickets for the luncheon are for sale (\$40) at the Registration Desk
Tuesday, 12:20 pm, April 10
Gallery Ballroom



Dave Robertson
GM Fellow/Analog Devices

Title: IC Technology and Innovation Life Cycles (or What Does It Take For My Paper to Get Accepted)

With decades of heroic effort -demanding cooperation across economic, social and national borders- the semiconductor industry has changed the course of human history and set mankind on a bold new path. Of course, analog circuit designers have done everything they could to prevent this.

The semiconductor industry may be "maturing," with increasing murmuring about the days of exponential innovation and explosive growth being over. The reality is more nuanced: there is still lots of room for invention, but we do acknowledge that certain technologies are "aging". However, even "mature" technical areas can experience a great deal of innovation, but the nature of the "breakthroughs" changes across a given technologies life cycle. This talk will reflect on these issues, with some particular examination of some mixed signal case studies (including data converters) and some reflection on the all important question of which papers are going to get into which conferences (and why).

Session 15 - Design Foundations for Advanced Technologies

Tuesday, April 10, 2:00 pm, Great Room 1-3

Session Chair: Paolo Miliozzi, Maxlinear
Session Co-Chair: Charles Augustine, Intel

This session focuses on design methodologies covering automated analog design, machine learning functional safety and reliability and provides a deep dive into design challenges at 7nm.

2:00pm **Introduction**

15-1
2:05 pm **Analog/Mixed-Signal Design Challenges in 7-nm CMOS and Beyond (Invited), (*Outstanding Invited Paper Nominee*)**, A.L.S. Loke, D. Yang, T.T. Wee, J.L. Holland, P. Isakanian, K. Rim, S. Yang, J.S. Schneider, G. Nallapati, S. Dundigal, H. Lakdawala, B. Amelifard, C.K. Lee, B. McGovern, P.S. Holdaway*, X. Kong, and B.M. Leary, Qualcomm Technologies, Inc., *Qualcomm, Inc

Smartphones with 7-nm SoCs are expected this year with 5 nm on the horizon. We summarize technology elements that enable 7-nm CMOS and beyond to address the impact on analog/mixed-signal design. We also present layout guidelines to reduce vulnerability to technology and model immaturity for early adopters of new nodes.

15-2
2:55 pm **BAG2: A Process-Portable Framework for Generator-Based AMS Circuit Design (Invited)**, E. Chang, J. Han, W. Bae, Z. Wang, N. Narevsky, B. Nikolić, E. Alon, UC Berkeley

We present BAG2, a framework for the development of process-portable Analog and Mixed Signal (AMS) circuit generators. We developed various complex circuit generators using BAG2, including a time-interleaved SAR ADC and a SerDes transceiver frontend. We verify our claims of process portability by presenting circuits generated in various technology nodes.

3:45 PM **BREAK**

15-3
4:00 pm **A 28nm FDSOI 8192-Point Digital ASIC Spectrometer from a Chisel Generator**, S. Bailey*, J. Wright*, N. Mehta*, R. Hochman*, R. Jarnot**, V. Milovanovic*, D. Werthimer*, B. Nikolic*, *UC Berkeley, ** NASA JPL

This work presents a Chisel ASIC spectrometer generator, which supports a wide array of applications through a modular and parameterized hierarchical design. Customizable features include filter coefficients, FFT bins, automatic pipelining, bitwidth selection with automatic bitwidth growth, and overall topology. An instance of the generator was selected, verified, and taped-out in a 28nm UTBB-FDSOI process to demonstrate its efficacy. Custom serial links bring high-speed data from a 3-bit external ADC to the digital spectrometer, which achieves a sample rate of 17 GS/s with an 8192-point FFT. Such a generator greatly simplifies ASIC spectrometer development, paving the way for future low-cost ASIC systems.

15-4
4:25 pm **Compact Modeling and Simulation of Accelerated Circuit Aging**, Devyani Patra, Jiayang Zhang*, Runsheng Wang*, Mehdi Katozzi**, Ethan H. Cannon**, Ru Huang*, Yu Cao, Arizona State University, *Peking University, **Boeing Research & Technology

Accelerated circuit aging is increasingly important at scaled technology, due to the feedback between circuit operation and reliability effects. This paper develops a compact model that is accurate and efficient in long-term prediction. The model is validated by data at 65nm, 28nm and 16/14nm, and demonstrated with various benchmark circuits.

15-5
4:50 pm **9.1x Error Acceptable Adaptive Artificial Neural Network Coupled LDPC ECC for Charge-trap and Floating-gate 3D-NAND Flash Memories, (*Outstanding Student Paper Nominee*)**, T. Nakamura, Y. Deguchi and K. Takeuchi, Chuo University

Adaptive Artificial Neural Network coupled (ANN) LDPC ECC is proposed to increase acceptable errors by 9.1-times for charge-trap and floating-gate 3D-NAND flash. Lateral charge migration, vertical charge de-trap, floating-gate capacitive coupling and word-line variations are automatically compensated. ANN precisely and adaptively estimates BER and memory cell errors are efficiently corrected.

15-6
5:15 pm **Functional Safety SoC for Autonomous Driving (Invited)**, Shinichi Shibahara, Renesas Electronics Corporation

This paper discusses two topics: implementation and verification for supporting functional safety. The SoC in this paper introduces safety mechanisms considering area and power constraints. The emulation of hardware built-in self-test in RTL simulation can improve the verification performance by 50 times, compared to gate level simulation with DFT-implemented netlist.

Session 16 - Cognitive Memories and Novel Accelerators

Tuesday, April 10, 2:00 pm, Great Room 4

Session Chair: Ken Takeuchi, Chuo University

Session Co-Chair: Rajiv Joshi, IBM T.J. Watson Research Labs

Memories for neuromorphic and in-process computation along with emphasis on ultra-low V_{min} memories for cognitive applications are presented. In addition, novel IoT sensor architecture which is smart, secured and energy efficient is presented along with accelerators for RNN, a high-performance, programmable lattice encryption instruction accelerator, and the first digital processor for always-on Binary Convolutional Neural Networks.

2:00pm **Introduction**

16-1
2:05 pm **RRAM Fabric for Neuromorphic and Reconfigurable Compute-in-memory Systems (Invited), (*Outstanding Invited Paper Nominee*)**, Mohammed A. Zidan, Wei D. Lu, University of Michigan, Ann Arbor

In this paper we discuss the development of resistive random-access memory (RRAM) devices and integrated systems for memory, bio-inspired neuromorphic computing, and arithmetic computing applications. A proposed structure that can enable dynamically reconfigurable systems (i.e. software-defined chips) based on a common physical fabric will also be introduced.

16-2
2:55 pm **Cascaded and Resonant SRAM Supply Boosting for Ultra-Low Voltage Cognitive IoT Applications**, R. V. Joshi, M. M. Ziegler, K. Swaminathan, N. Chandramoorthy, IBM T. J. Watson Research Center

To enable ultra-low power cognitive IoT systems, we present novel supply boosting techniques allowing low voltage SRAM. These techniques include enhancements at both the device and circuit levels. A new 14nm SOI test chip employing the techniques shows functional 8T SRAM down to 0.24V. We also show how supply boosting can lead to lower voltage operation of cognitive IoT applications using an example of a neural network running the MNIST benchmark.

16-3
3:20 pm **Chipmunk: A Systolically Scalable 0.9 mm², 3.08 Gop/s/mW @ 1.2 mW Accelerator for Near-Sensor Recurrent Neural Network Inference**, Francesco Conti*, Lukas

Cavigelli**, Gianna Paulin**, Igor Susmelj**, Luca Benini*, *ETH Zurich & University of Bologna, **ETH Zurich

Here we present Chipmunk, a small (<1mm²) hardware accelerator for Long-Short Term Memory RNNs in UMC 65nm technology capable to operate at a measured peak efficiency up to 3.08 Gop/s/mW. An architecture with 75 equal Chipmunk tiles can achieve real-time phoneme extraction on a demanding RNN topology consuming <13mW average power.

3:45 PM **BREAK**

16-4
4:00 pm **Simultaneously Ensuring Smartness, Security, and Energy Efficiency in Internet-of-Things Sensors (Invited)**, A. O. Akmandor, H. Yin, N. K. Jha, Princeton University

Internet-of-Things sensors pose significant design challenges: limited bandwidth, insufficient energy, and security flaws. Due to their inherent trade-offs, these design challenges have not yet been simultaneously addressed. We propose a novel way out of this predicament by employing signal compression, machine learning inference, and cryptographic techniques on the IoT sensor.

16-5
4:50 pm **LEIA: A 2.05mm² 140mW Lattice Encryption Instruction Accelerator in 40nm CMOS**, S. Song, W. Tang, T. Chen, Z. Zhang, University of Michigan

This work presents LEIA, a high-performance, programmable lattice encryption instruction accelerator that supports all published ring learning with errors schemes. LEIA is prototyped in a 2.05mm² 40nm CMOS chip, and it achieves up to three orders of magnitude improvement in performance and energy efficiency in core operations over state-of-the-art designs.

16-6
5:15 pm **BinarEye: An Always-On Energy-Accuracy-Scalable Binary CNN Processor With All Memory On Chip In 28nm CMOS**, B. Moons*, D. Bankman**, L. Yang**, B. Murmann**, M. Verhelst*, *ESAT-MICAS, KU Leuven, Leuven, Belgium, **Stanford University, Stanford, CA, USA

BinarEye is an always-on Binary CNN processor. It is memory-like, requires no off-chip bandwidth and can trade energy for accuracy. It shows full-system input-to-label efficiencies of 230 1b-TOPS/W and consumes 14.4uJ/f on 86%/CIFAR10 down to 0.92uJ/f for 94%/face detection. This is 3-12-70x better than the SotA at on par accuracy.

Session 17 - Panel-What is the Sweet Spot of Voltage Regulator Integration

Tuesday, April 10, 2:00 pm, Great Room 5

Chairs: Patrick Mercier, UCSD and Zeynep Deniz, IBM

Vivek De, Intel
Seth Sanders, UC Berkeley

David Giuliano, Peregrine
Philip Mok, HKUST

The mismatch between voltages produced by high-density batteries and the supply voltage needs of scaled CMOS SoCs necessitates DC-DC converter integration in essentially all modern electronic devices. Conventionally, large off-chip power management integrated circuits (PMICs) are used to generate one or more fixed rails for each SoC domain. However, the constituent passives (inductors and capacitors) consume large board area and volume in tightly integrated mobile devices, and large PMICs have difficulty supporting fine-grain dynamic voltage scaling needed in modern SoCs. This panel will introduce and debate the various merits of various state-of-the-art power management options, including hybrid inductive/capacitive converter topologies, integrated inductors, switched-capacitor converters, distributed LDOs, all-digital regulators, and more. Will a winning approach emerge? Attend to find out!

3:45 PM **BREAK**

Session 18 - Wireline Transceivers and Building Blocks

Tuesday, April 10, 2:00 pm, Great Room 6-8

Session Chair: Tod Dickson, IBM T.J. Watson Research Labs

Session Co-Chair: Mayank Raj, Xilinx

This session introduces innovations in ultra-high-speed and low-power wireline links. Advancements in CDRs, transmitters, equalizers, single-ended signaling, and optical receivers will be presented.

2:00pm **Introduction**

18-1 **A 3.125-to-28.125 Gb/s Multi-Standard Transceiver with a Fully Channel-independent Operation in 40nm CMOS**, J. H. Yoon, K. Kwon, H. M. Bae, KAIST
2:05 pm

The proposed CDR IC achieves wide tuning range with low clock jitter because a ring oscillator in each channel is injection-locked to a global LC VCO. Each CDR lane generates a channel-independent injection clock using a variable clock divider, a highly linear phase rotator, and a frequency tracking loop.

18-2 **A 25Gb/s APD-Based Burst-Mode Optical Receiver with 2.24ns Reconfiguration Time in 28nm CMOS**, K.-C. Chen, A. Emami, California Institute of Technology
2:30 pm

This paper describes an avalanche photodetector based burst-mode optical receiver in 28nm CMOS, incorporating equalizations to improve speed and sensitivity, and integrating DC and amplitude comparators to reduce reconfiguration time. The receiver achieves -16dBm sensitivity, 2.24ns reconfiguration time with 5dB dynamic range, and 1.37 pJ/bit energy efficiency at 25Gb/s.

18-3 **A 32-mW 40-Gb/s CMOS NRZ Transmitter**, Yikun Chang, Abishek Manian, Long Kong, Behzad Razavi, University of California, Los Angeles
2:55 pm

A wireline transmitter with 2-tap feedforward equalization achieves more than a two-fold improvement in the power efficiency through the use of a new integrating multiplexer, as well as quadrature clock phases with 25% duty cycle. Serializing data by a factor of 128 and including an on-chip phase-locked loop, the transmitter is realized in 45-nm CMOS technology and delivers a differential output swing of 460 mVpp.

18-4 **A 56 Gb/s 6 mW 300 μm^2 inverter-based CTLE for short-reach PAM2 applications in 16 nm CMOS**, Kevin Zheng*, Yohan Frans**, Ken Chang**, Boris Murmann*, *Stanford University, **Xilinx Inc.
3:20 pm

A 56 Gb/s inverter-based CTLE in 16 nm CMOS is implemented for a short-reach transceiver, achieving 31% UI margin for an 8 dB loss channel. A ring oscillator based LDO biases the inverters for PVT variations. The CTLE core measures only 20 μm x 15 μm and consumes 6 mW

3:45 PM **BREAK**

18-5 **Ground-Referenced Signaling for Intra-Chip and Short-Reach Chip-to-Chip Interconnects (Invited), (Outstanding Invited Paper Nominee)**, Walker J. Turner, John W. Poulton, John M. Wilson, Xi Chen, Stephen G. Tell, Matthew Fojtik, Thomas H. Greer III, Brian Zimmer, Sanquan Song, Nikola Nedovic, Sudhir S. Kudva, Sunil R. Sudhakaran,
4:00 pm

Rizwan Bashirullah*, Wenxu Zhao**, William J. Dally, C. Thomas Gray, NVIDIA, *University of Florida, **Broadcom

Ground-referenced signaling solves many of the problems of single-ended signaling systems and can be adapted for RC-dominated channels and LC transmission lines. Multiple generations of GRS-based serial links are presented, including a 16Gb/s 170fJ/b/mm on-chip link, a 20Gb/s 0.58pJ/b link across an organic package, and a 25Gb/s 1.17pJ/b link over a printed-circuit board.

18-6
4:50 pm **A 15Gb/s 1.9pJ/bit Sub-baud-rate Digital CDR, (*Outstanding Student Paper Nominee*)**, D. Kim, W. Choi, A. Elkholy, J. Kenney*, P. Hanumolu, University of Illinois at Urbana-Champaign, *Analog Devices Inc.

A sub-baud-rate CDR that can recovery clock and data using only a quarter-rate clock is presented. Four data bits are recovered in each clock cycle using eight samplers and a current integrator. Four of the eight samplers used for data recovery are re-used for phase detection. Fabricated in a 65nm CMOS process and operating with 11dB channel loss, the prototype CDR recovers 15.2Gb/s data using a 3.8GHz clock and achieves BER < 10^{-12} , > 10MHz JTOL corner, 548fs_{rms} recovered clock jitter, and 1.9pJ/bit energy efficiency.

Session 19 - Power Management Techniques Energy Harvesting

Tuesday, April 10, 4:00 pm, Great Room 5

Session Chair: Mehdi Kiani, Pennsylvania State University

Session Co-Chair: Stefano Pietri, NXP Semiconductors

Novel circuit and system techniques for efficient RF, vibration and thermal energy harvesters will be presented in this session.

3:55 pm **Introduction**

19-1
4:00 pm **A Low-power Integrated Power Converter for an Electromagnetic Vibration Energy Harvester with 150 mV-AC Cold Startup, Frequency Tuning, and 50 Hz AC-to-DC Conversion**, Ujwal Radhakrishna, Patrick Riehl*, Nachiket Desai, Phillip Nadeau, Yuechen Yang, Abraham Shin, Jeffrey H. Lang, Anantha P. Chandrakasan, Massachusetts Institute of Technology,*Analog Devices, Inc.

This paper demonstrates the first fully functional power converter designed to interface a MEMS-based electromagnetic (EM) vibration energy harvester for near-50 Hz vibrational machine health monitoring. The IC accomplishes (i) cold-start from 50 Hz-150 mV-peak AC input to 1.1 V output, (ii) conjugate impedance matching for maximum power extraction along with resonant frequency tuning and (iii) input-AC to output- DC voltage conversion. Cold-startup is achieved using an on-chip Meissner oscillator with an off-chip transformer. Thereafter, a self-timed current-feedback-based H-bridge circuit is turned on for conjugate impedance matching with on-chip control and an off-chip microcontroller for impedance synthesis. The regularoperation H-bridge circuit delivers 820 uW to load capacitor at 71% efficiency at resonance. It also does frequency tuning to deliver 650 uW at off-resonance, thereby demonstrating robustness to possible harvester-resonance variations because of manufacturing tolerances. This makes it the first-demonstration of a full-system low-power interface IC for vibrational harvesters. The prototype is fabricated in 0.18 um CMOS process and has an active area of 1.5 mm².

19-2
4:25 pm **A 14 nA Quiescent Current Inductorless Dual-Input-Triple-Output Thermoelectric Energy Harvesting System Based on a Reconfigurable TEG Array**, Q.Wan, P.K.T. Mok, The Hong Kong University of Science and Technology

This paper presents an inductorless dual-input-triple-output thermoelectric energy harvesting system with 14 nA quiescent current based on a reconfigurable TEG array. Higher than 85% efficiency can be achieved over an input voltage range of 0.15V-to-10.8V and an output power range of 38 μ W-to-200mW with 99% peak efficiency.

19-3
4:50 pm **Fully-Integrated 57 mV Cold Start of a Thermoelectric Energy Harvester using a Cross-Coupled Complementary Charge Pump**, S. Bose, T. Anand, and M.L. Johnston, Oregon State University

This paper presents an integrated cold-start architecture for thermoelectric energy harvesters comprising a novel cross-coupled complementary charge pump with clocks generated by an ultra-low voltage ring oscillator to achieve start-up at 57mV in 135ms. This is the lowest reported start-up voltage to date for fully-integrated cold-start of a thermoelectric harvester.

19-4
5:15 pm **A Fully Integrated 28nm CMOS Dual Source Adaptive Thermoelectric and RF Energy Harvesting Circuit with 110mV Startup Voltage**, Yi-Wu Tang, Chien-Heng Wong, Yuan Du, Li Du, Yilei Li, Mau-Chung F. Chang, UCLA

A fully integrated dual source adaptive thermoelectric and RF energy harvesting circuit is presented. Its boost oscillator, rectifier and boost converter all operate at RF frequency to make inductor and capacitor integration feasible. The oscillator Gm adaptive bias reduces current consumption at higher voltage while assisting startup at lower voltage. The RF input signal further reduces startup voltage through Q-enhanced amplification and super-regenerative mode. Implemented in 28nm CMOS, the self-startup voltage was 110mV without RF input and 85mV at -16dBm input. The boost converter peak output power is 520uW, power conversion efficiency (PCE) is 25% and end-to-end PCE is 10%.

19-5
5:40 pm **A 5 μ W-5mW Input Power Range, 0-3.5V Output Voltage Range RF Energy Harvester with Power-Estimator-Enhanced MPPT Controller**, X. Hua, R. Harjani, University of Minnesota

A 5 μ W - 5mW input power range, 0 - 3.5V output voltage range RF energy harvester is designed to charge supercapacitors for RFID applications. Voltage protection techniques are used to improve the peak output voltage from 2.5V to 3.5V resulting in a 100% increase in stored energy. An all analog low power maximum power point tracking (MPPT) controller with an embedded power estimator increases the maximum tracking speed by 8x, improves the input power range by 8x, and accumulates 35% more energy during charging transients. The chip is fabricated in TSMC's 65nm GP process, occupies an area of 0.15mm², and has a measured peak efficiency of 91%.

Session 20 - Oversampling A/D Converters

Wednesday, April 11, 8:30 am, Great Room 1-3

Session Chair: Nima Maghari, University of Florida

Session Co-Chair: Baradwaj Vignanam, Maxlinear

This session presents several oversampling A/D converters with bandwidths ranging from 25kHz to 200 MHz enabled by a variety of circuit-level and system level techniques.

8:30 am **Introduction**

20-1
8:35 am **Finite-Impulse-Response (FIR) Feedback in Continuous-Time Delta-Sigma Converters (Invited), (*Outstanding Invited Paper Nominee*)**, S.Pavan, Indian Institute of Technology, Madras

Finite-impulse-response (FIR) feedback was originally introduced as a way to address the problem of clock jitter in continuous-time delta-sigma modulators. It turns out that FIR feedback has many other benefits -- it relaxes linearity requirements of the modulator's loop filter, reduces the effect of the quantizer's data-dependent jitter and enables the use of chopping "for free". It can be thought of as an architectural technique that combines the benefits of single-bit and multibit operation. It has proven itself to be a robust and scalable technique, applicable to delta-sigma data converters targeting a variety of specifications, and across process nodes. This paper reviews the key challenges encountered in the design of high performance delta-sigma data converters, and describes the role of FIR feedback in addressing these challenges. Recent research in this area and promising directions are reviewed.

20-2
9:25 am

An 85MHz-BW 68.5dB-SNDR ASAR-Assisted CT 4-0 MASH $\Delta\Sigma$ Modulator with Half-Range Dithering-Based DAC Calibration in 28nm CMOS, H. Liu, G. Gielen, KU Leuven, X. Xing, Tsinghua University

This paper presents an on-chip half-range dithering-based calibration technique for the current-steering feedback DAC in an ASAR-assisted continuous-time 4-0 MASH $\Delta\Sigma$ modulator achieving 85MHz BW 68.5dB SNDR. The proposed calibration randomizes the DAC cells and effectively improves the modulator's SFDR, with limited overhead cost in terms of area and power consumption.

20-3
9:50 am

A 1V 175uW 94.6dB SNDR 25kHz Bandwidth Delta-Sigma Modulator Using Segmented Integration Techniques, Sheng-Hui Liao, Jieh-Tsong Wu, National Chiao Tung University

A 2-1 MASH SC-DSM using segmented integration techniques is presented. We constantly alternate the circuit configurations of its internal integrators to optimize power consumption. The integrators are accelerated only when they are in crucial integration cycle. It achieves 94.6dB SNDR in a 25kHz signal bandwidth, while only consuming 175uW.

10:15 AM

BREAK

20-4
10:40 am

A Continuous-Time Delta-Sigma Modulator with Self-ELD Compensated Quantizer, C. Han, T. Kim*, and N. Maghari, University of Florida, *Now with Microchip Technology Inc.

A new excess loop delay (ELD) compensation technique, self-ELD compensation, is proposed. The digital output is stored on the input parasitic capacitance of a comparator and used to perform ELD compensation. No extra circuit, such as opamp or DAC, is required, since the proposed method uses the existing circuit component.

20-5
11:05 am

A 200MHz-BW 0.13mm² 62dB-DR VCO-Based Non-Uniform Sampling ADC with Phase-Domain Level Crossing in 65nm CMOS, (*Outstanding Student Paper Nominee*), Tzu-Fan Wu, Mike Shuo-Wei Chen, University of Southern California

This paper introduces a VCO-based non-uniform sampling ADC that leverages phase-domain level crossing and VCO linearity calibration. The SQNR is improved by first-order noise shaping and inherent dithering via non-uniform oversampling. This ADC achieves 200MHz BW and 62dB DR with an active area of 0.13mm² in 65nm CMOS.

20-6
11:30 am

A 1 MHz Bandwidth, Filtering Continuous-Time Delta-Sigma ADC with 36 dBFS Out-of-Band IIP3 and 76 dB SNDR, S.Manivannan, S.Pavan, IIT Madras

The high dynamic range of CTDSMs used in wireless receivers, needed to accommodate large out-of-band interferers, can be reduced by using a filter up front. Embedding the filter inside the modulator loop is more power efficient. Prior work has embedded a Tow-Thomas biquad inside the ADC. We show that using a Rauch filter instead yields higher out-of-band linearity (for the same power dissipation) due to the passive-RC filtering inherent in the Rauch structure. The theory is borne out by measurements from a 1 MHz bandwidth CTDSM with an embedded second-order Rauch filter, achieving 76 dB SNDR and 36 dBFS out-of-band IIP3 while consuming 2.2mW in a 65nm CMOS process.

Session 21 - Timing Techniques

Wednesday, April 11, 8:30 am, Great Room 4

Session Chair: Zhenqi Chen, Qualcomm

Session Co-Chair: Fahran Adil, MIT Lincoln Labs

This session includes advanced timing techniques focusing on a bw jitter PLL, oscillators, and a low power time-to-digital converter.

8:30 am **Introduction**

21-1
8:35 am **A 0.008mm² 2.4GHz Type-I Sub-Sampling Ring-Oscillator-based Phase-Locked Loop with a -239.7dB FoM and -64dBc Reference Spurs, (*Outstanding Student Paper Nominee*),** Shravan S. Nagam, Peter R. Kinget, Columbia University

A ring-oscillator (RO) based PLL is presented combining a type-I architecture and a sub-sampling phase detector (SSPD). It achieves low jitter thanks to the wide-bandwidth type-I loop and low reference spurs thanks to the SSPD with its sample-and-hold function and high gain. The integrating filter capacitor is avoided, resulting in very low area. The RO PLL prototype in 65nm CMOS occupies 0.008mm², has a loop bandwidth of 15MHz and tunes from 2 to 3.2GHz. It consumes 6.1mW at 2.4GHz with a phase noise of -122.6dBc/Hz at 1MHz offset. The measured reference spurs, RMSjitter and FoMjitter are -64.2dBc, 422fs and -239.7dB.

21-2
9:00 am **A 46μW, 8.2MHz Self-threshold-tracking Differential Relaxation Oscillator with 7.66psrms Period Jitter and 1.56ppm Allan Deviation Floor,** Shao-Lung Lu, Yu-Te Liao, National Chiao Tung University

This paper presents an 8.2MHz relaxation oscillator with swing boosting and self threshold tracking techniques, designed to improve both period jitter and frequency stability. A self-threshold-tracking loop ensures the switching threshold is kept in a constant, reducing the frequency uncertainty from process, temperature and supply voltage variations. Implemented in a 180nm CMOS process, the design achieves a period jitter of 7.66psrms, an Allan deviation floor of 1.56ppm, a temperature coefficient of 123ppm from -20 to 100°C, and an FOM of over 160dBc/Hz while only consuming 46.3μW. The power efficiency of the design is 5.6kHz/nW.

21-3
9:25 am **A 350-mV, Under-200-ppm Allan Deviation Floor Gate-Leakage-Based Timer Using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS,** A. Kobayashi*, Y. Nishio*, K. Hayashi*, K. Nakazato*, K. Niitsu* **, *Nagoya University, **JST/PRESTO

This paper presents a gate-leakage-based timer using an amplifier-less replica-bias switching technique that can realize stable and low-voltage operation with logic circuits based architecture. The test chip achieves an energy efficiency of 25pJ/cycle at a supply voltage of 350mV, and 200-ppm Allan deviation floor.

21-4
9:50 am **A 78.2nW 3-Channel Time-Delay-to-Digital Converter using Polarity Coincidence for Audio-based Object Localization**, Daniel de Godoy, Xiaofan Jiang and Peter R. Kinget, Columbia University

A polarity-coincidence based adaptive time-delay estimation is introduced for ultra-low-power analog-to-feature conversion. A 0.18um CMOS prototype with four analog input channels and three 8-bit digital output delays consumes 78.2nW while operating at 50KHz with 20us TLSB and 6.06 ENOB. This analog-to-feature converter is demonstrated in an audio-based vehicle-bearing-estimation IoT application.

10:15 AM **BREAK**

Session 22 - Forum-Device and Integration at Advanced Technology Nodes

Wednesday, April 11, 8:30 am, Great Room 5

Forum Chairs: Asif Khan Georgia Tech, and Harish Krishnamurthy Intel

8:30 am **Introduction**

8:35 am **Energy efficient computing and sensing with Tunnel FETs**, Adrian Ionescu, EPFL
22-1

9:05 am **Forget about SoCs lets talk SoWs - Systems-on-Wafers**, Subramanian, S. Iyer,
22-2
UCLA

9:35 am **Multi-Die Heterogeneous Integration using Interconnect Stitching for the Next Era of Moore's Law**, Muhannad Bakir, Georgia Tech
22-3

10:05 am **Moore's Law to Application driven Technology Development**, Titash Rakshit,
22-4
Samsung

Session 23 - Low-Power Radios for IoT and Medical Connectivity

Wednesday, April 11, 8:30 am, Great Room 6-8

Session Chair: Hossein Miri Lavasani, Qualcomm

Session Co-Chair: Yahya Tousi, University of Minnesota

This session covers advances in the design and low-power wireless transceivers for IoT and medical implants.

8:30 am **Introduction**

23-1
8:35 am **Wireless Data Links for Next-Generation Networked Micro-Implantables (Invited)**,
Max L. Wang, Spyridon Baltasavias, Ting Chia Chang, Marcus J. Weber, Jayant Charthad,
Amin Arbabian Stanford University

This paper reviews electromagnetic and ultrasonic communication links for miniaturized implants. Electromagnetic links have demonstrated high data rates, limited to tissue depths under 5 cm. Ultrasonic links have shown deeper transmissions, but with limited data rate. Spatial multiplexing is proposed to increase ultrasonic capacity without additional power or bandwidth.

23-2
9:25 am **A 100 kb/s, 4 GHz, 267 μW Fully Integrated Low Power FM-UWB Transceiver with Multiple Channels**, V. Kopta* **, C.ENZ**, *EPFL, **CSEM

A 4 GHz FM-UWB transceiver is presented. Two receivers and a transmitter reuse a single port, without the need for external components. Receiver consumes 267 μ W in low-power mode, and provides 4 FDMA channels in the multi-user mode at 550 μ W. Transmitter consumes 575 μ W at -11.4 dBm output power.

23-3
9:50 am **A Fully Integrated Multi-Mode High-Efficiency Transmitter for IoT Applications in 40nm CMOS**, M. Sharifzadeh, A. Masnadi-Shirazi, Y. Rajavi, H. Lavasani, M. Taghivand, Qulacomm Inc.

This paper presents a fully integrated multi-mode high-efficiency transmitter, employing supply scaling technique using a DC-DC converter to improve the efficiency for IoT applications. The proposed architecture improves the efficiency of the conventional constant-supply switching PAs by a factor of 3 and achieves power saving of nearly 1mW with 1.6mW power consumption at -10dBm, which is the lowest reported power consumption in the literature.

23-4
10:15 am **A -80dBm BLE-compliant, FSK Wake-up Receiver with System and Within-bit Duty Cycling for Scalable Power and Latency**, M. R. Abdelhamid, A. Paidimarri*, A. P. Chandrakasan, MIT, *IBM T. J. Watson Research Center

This paper presents a multimode -80dBm sensitivity wake-up receiver with a BLE-compatible event-driven low power mode consuming 240nW while a BLE low latency mode can wake up in 200 μ s at a 230 μ W consumption. A custom FSK transmission mode can trigger wake-up at 17nW for an average latency of 5 seconds.

Session 24 - Panel-Is the IC Startup Era Over or Just Transitioning

Wednesday, April 11, 11:00 am, Great Room 5

Chairs: Hanh-Phuc Le, U. of Colorado Boulder, and Rikky Muller, UC Berkeley

Benton Calhoun, Professor, University of Virginia and PsiKick
Karim Arabi, Atlazo

Richard Schwerdtfeger, NSF
Wonyoung Kim, Lion Semiconductor
Shahin Farshchi, Lux Capital

With a thirst for improving lives and changing the world, semiconductor startups, fueled by novel technical ideas, ambitious business plans, speed, agility and risk, played a key part in forming the famous Silicon Valley in California. The resulting high returns and benefits to the society inspired VC, investors, government agencies to increase their funding for new startups. However, it seems much harder to secure investments for semiconductor startups recently compared with the golden age of IC startups in 2000s. Is the IC startup era coming to an end, or just transitioning to new models? If so, what are they? The discussion in this panel will cover many different perspectives of the carefully selected panelists, including a famous IC professor with years of startup experience, a large-firm-VP-turned-startup founder, an 8-figure-funded startup CEO with fresh PhD, an NSF SBIR program director with semiconductor portfolio, and a VC with a long list of successful semiconductor investments.

Session 25 - Panel-What can/should Circuit Designers do to Ride on the Wave of Machine Learning

Wednesday, April 11, 11:00 am, Great Room 6-8

Chair: Mike Chen, USC, and John Khoury, Silicon Labs

Boris Murmann, Stanford
Edgar Sanchez-Sinencio, TAMU

Mingoo Seok, Columbia University
Vivek De, Intel

Analog neural networks were a hot research topic in the late 1980s but fell out of favor after a few years. Now, 25 years later, neural networks/Machine Learning has returned in force with impressive real world results. Machine learning has been resurging thanks to the large quantity of available data on the cloud. These modern neural networks are being implemented on GPUs. Will analog neural networks or even a hybrid approach yield important benefits over and above GPU implementations? How can analog circuit designers contribute to this new wave? What direction should we take? How should we re-educate ourselves? In this panel, we assemble a group of analog and digital circuit researchers as well as industry professionals to share their views on this potential opportunity.

Closing and Awards Ceremony

Wednesday, April 11, 1:30 pm-2:30 pm, Gallery

General Information

LOCATION

DoubleTree Mission Valley, 7450 Hazard Center Drive, San Diego, CA, 92108

Telephone: +1-619-297-5466

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REGISTRATION

Payment of the Technical Session registration fee entitles the registrant to entrance to the Sunday Educational Sessions and the Monday-Wednesday Technical Sessions, Monday's Welcome Reception, Tuesday's Conference Reception, and to one copy of the flash drive of the technical papers.

Single-day registration (Sunday Educational Session, Monday, Tuesday or Wednesday Technical Sessions) entitles the registrant to that day's events only and one copy of the flash drive of the technical papers.

Questions on Your Registration

If you have questions on your registration, please contact:

By email: melissaw@widerkehr.com

By phone: 301-527-0900 x 1, By fax: 301-527-0994

Onsite Registration and Advance Registration Badge Pick-Up

The Registration Center, located in the Great Room Foyer, will be open as follows:

| | |
|---------------------|--------------------|
| Sunday, April 8 | 7:00 am - 5:00 pm |
| Monday, April 9 | 7:30 am - 5:00 pm |
| Tuesday, April 10 | 8:00 am - 5:00 pm |
| Wednesday, April 11 | 8:00 am - 11:00 am |

WELCOME RECEPTION AND CONFERENCE RECEPTION

Welcome Reception – Monday Evening, April 9, 5:30 pm - 7:00 pm

Gallery Ballroom

The first CICC social event this year is the Welcome Reception. All conference attendees are cordially invited!

Conference Reception – Tuesday. Evening, April 10, 5:30 pm – 7:00 pm

Gallery Ballroom

Join the CICC for a Tuesday night reception.

CICC KEYNOTE LUNCHEON

Tickets for the luncheon are for sale at the Registration Desk

Tuesday, 12:20 pm, April 10

Gallery Ballroom



Dave Robertson
GM Fellow/Analog Devices

Title: IC Technology and Innovation Life Cycles (or What Does It Take For My Paper to Get Accepted)

With decades of heroic effort -demanding cooperation across economic, social and national borders- the semiconductor industry has changed the course of human history and set mankind on a bold new path. Of course, analog circuit designers have done everything they could to prevent this.

The semiconductor industry may be "maturing," with increasing murmuring about the days of exponential innovation and explosive growth being over. The reality is more nuanced: there is still lots of room for invention, but we do acknowledge that certain technologies are "aging". However, even "mature" technical areas can experience a great deal of innovation, but the nature of the "breakthroughs" changes across a given technologies life cycle. This talk will reflect on these issues, with some particular examination of some mixed signal case studies (including data converters) and some reflection on the all important question of which papers are going to get into which conferences (and why).

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The proceedings USB contains papers on each presentation. Technical Session registrants will receive one flash drive of the Proceedings. Additional copies of the flash drive can be purchased onsite at the conference registration desk, IEEE member: \$80, Non-member: \$90. Flash drives are not for sale by IEEE after the conference.

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Badges are required for admittance to all sessions and the exhibit hall. Please wear your badge at all times while attending the conference so that you will not be delayed entry to a session.

FOR FURTHER INFORMATION CONTACT

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