

**CICC Technical Program  
Monday - Wednesday**

**Session 1 - Plenary**

Monday, May 1, 8:00 - 9:30, Lady Bird 1 Ballroom

1-1 **Autonomy with Smart Power Electronics**, Hans Stork, ON Semiconductor



The next decade will likely see the arrival of many autonomously moving devices. From humanoid-like robots that walk and talk, to self-driving cars, and to delivering drones. All enabled by sensors (position, movement, light, chemical), actuators (motors, levers, displays), and local as well as cloud-based intelligence. Most of these based on semi-conductor devices and technology.

Movement requires force, work and power, and the semiconductor devices that can deliver and transform sufficient energy are built using very different dimensions and process integration than the digital electronics used for computing and control. Bringing these two worlds together in small form factors requires heterogeneous integration or packaging, called modules.

Recent progress in the power / volume, efficiency, and intelligence of modules has accelerated through much progress in the active devices, but also from substrate and package capabilities. Scaling power devices for lower cost and higher efficiency has been accomplished with trench based architectures, super-junction doping profiles, and ultra-thin wafer processes. Recent generations of IGBTs and power MOSFETs achieve on resistances and operating frequencies at tighter densities than ever, leading to much discussion about their ultimate limits, not unlike the prognostications in advanced logic technology. And if Silicon cannot be extended further, there are the wide bandgap materials of GaN and SiC to extend voltage, speed, or temperature. Especially promising is the system level benefit of higher frequency operation. With smaller coils and capacitors, much smaller form factors can be achieved, all essential factors for autonomous mobility.

Co-packing all these unique components is enabled by progress in substrates with thinner, finer interconnect, yet with adequate heat dissipation from better materials choices. While the IQ of intelligent power modules has increased cost / performance in many fields, nowhere has the progress of 3D integration been more impressive than in image sensors. Here, use of wafer level stacking allows better optimization of the sensor layers, the analog transfer functions, and the digital image processing. Add to this the wafer level processes for lenses and focus techniques, and miniature imaging devices are a common reality, dealing now with extreme dynamic range and robustness requirements from the automotive world. The required intelligence for decision making at highway speeds is core to realizing the autonomous driving experience.

In this talk, we will cover the range of technical trade-offs encountered in scaling power devices, realizing the potential of wide bandgap materials through adjusted circuit topologies, and the challenges of heterogeneous packaging and integration. At last, after many decades of exponential progress in logic and memory technologies, the “real world” devices of power handling and sensor functions are jointly enabling another wave of electronics progress, namely all things autonomously moving.

## Session 2 - Wireline Techniques for Advanced Modulation Schemes

Monday, May 1, 10:00 – 12:00, Lady Bird 1 Room  
Session Chair: Sudip Shekhar, University of British Columbia  
Session Co-Chair: Tod Dickson, IBM

This session presents a 64Mb ReRAM with reliable RD/WR operations, offset-cancelling sense-amplifier for ReRAM, value-aware vertical 3D TLC NAND flash memory, and adaptive circuit assists for enabling SRAM operation at NTV.

10:00 am      **Introduction**

10:05 am      **A Supposedly Clever Thing I'll Never Do Again (Invited)**, Aaron Buchwald, Inphi  
2-1

This paper will review a few “clever” ideas with disappointing results, focusing primarily on the use of a slow, but accurate, reference ADC for system-identification approaches to background calibration in time-interleaved ADCs, where complications ultimately limit performance in a variety of unanticipated ways.

10:55 am      **Channel Adaptive ADC and TDC for 28 Gb/s 4pJ/bit PAM-4 Digital Receiver**,  
2-2      Aurangozeb, AKM Delwar Hossain, Masum Hossain, University of Alberta

A low power channel adaptive 28 Gb/s PAM-4 receiver utilizes a predictive 2-to-5.5-bit ADC, a 5-bit SAR TDC, and a 3-to-8 programmable tap FFE in digital domain. Measured power consumption is 130mW(excluding DSP). The receiver enables energy proportional loss compensation with average energy efficiency better than 4 pJ/bit including DSP.

11:20 am      **A 4-40 Gb/s PAM4 Transmitter with Output Linearity Optimization in 65 nm CMOS**,  
2-3      Xuqiang Zheng, Chun Zhang, Fangxu Lv, Feng Zhao, Shigang Yue, Ziqiang Wang\*, Fule Li\*, Hanjun Jiang\*, and Zhihua Wang\*, Tsinghua University, \*University of Lincoln

This paper presents a 4-40Gb/s current mode PAM4 transmitter in 65nm CMOS. By embedding current-compensating circuits into the output driver and developing a coherent scaled-replica based bias generator, the peak-to-peak swing achieves 960mV with an eye linearity of 1.01 in AC coupling mode.

11:45 am      **A 10-to-650MHz 1.35W Class-AB Power Amplifier with Instantaneous Supply-Switching Efficiency Enhancement**, J. Lee, S. Pamarti, R. Gomez\*, UCLA, \*Broadcom  
2-4      Ltd.

A novel PA supply-modulation technique is introduced. Cascode transistors switch output signal current to high/low supply rails depending on instantaneous amplitude. GHz-rate current-mode switching enhances efficiency for bandwidths beyond existing envelope trackers. 1.35W peak power and efficiency=13.6%@11dB PAPR are observed. Combined Pout, fractional bandwidth and high-PAPR efficiency exceed prior art.

## Session 3 - Clocking Techniques

Monday, May 1, 10:00 - 12:00, Lady Bird 2 Room  
Session Chair: Sudhakar Pamarti, UCLA  
Session Co-Chair: Nan Sun, University of Texas

This session includes advanced clocking techniques focusing on jitter/noise/spurious tone reduction in phase lock loops implemented in finely scaled CMOS processes.

10:00 am      **Introduction**

10:05 am      **A 0.951 Ps<sub>rms</sub> Period Jitter, 3.2% Modulation Range, DSM-Free, Spread-Spectrum PLL**, H. Sun, K. Sobue\*, K. Hamashita\*, T. Anand, and U. Moon, Oregon State University, \*Asahi Kasei Microdevices  
3-1

This work presents a DSM-free spread-spectrum PLL. The proposed charge-based discrete-time loop filter enables wide and PVT-insensitive modulation. Correlated double sampling minimizes noise penalty. This work achieves 3.2% spread-spectrum modulation range with 26.51dB attenuation. Implemented in 0.18 $\mu$ m CMOS, this work achieves 951fsrms period jitter while consuming 9.93mW from 1.8V supply.

10:30 am      **A 0.031mm<sup>2</sup>, 910fs, 0.5-4GHz Injection Type SOC PLL with 90dB Built-in Supply Noise Rejection in 10nm FinFET CMOS**, Chin-Yang Wu, Ruel-Pin Shen, Chih-Hsien Chang, Kenny Hsieh, Mark Chen, TSMC  
3-2

This paper presents a wide operating range (0.5~4GHz) PLL using soft injection techniques. Its ring-type VCO achieves built-in 90dB PSRR. This design achieves 910fs RMS phase jitters and -58dBc/Hz reference spur of a 3GHz output. The prototype PLL is fabricated in 10nm Fin-FET process with an active area of 0.031mm<sup>2</sup>.

10:55 am      **A -236.3dB FoM Sub-Sampling Low-Jitter Supply-Robust Ring-Oscillator PLL for Clocking Applications with Feed-Forward Noise-Cancellation**, Shravan S. Nagam, Peter R. Kinget, Columbia University  
3-3

A 2-2.8GHz 65nm CMOS ring oscillator PLL occupies an active area of 0.022mm<sup>2</sup>, consumes 5.86mW and achieves a 633fs RMS jitter at 2.36 GHz and an FOMjitter of -236.3dB. It implements a low-overhead feed-forward phase and supply-noise cancellation scheme by leveraging the noise extraction inherently done by the sub-sampling phase detector. Cancellation reduces the jitter by 1.4x, the phase noise by 10.2dB to -123.5dBc/Hz at a 300KHz offset, and the ring oscillator supply sensitivity by 19.5dB for a 1mVp-p 100KHz supply noise tone.

11:20 am      **Second and Third-Order Successive Requantizers for Spurious Tone Reduction in Low-Noise Fractional-N PLLs**, E. Familier, I. Galton, University of California, San Diego  
3-4

This paper presents 2nd- and 3rd-order digital requantizers which can be used as drop-in replacements for digital delta-sigma modulators in analog fractional-N PLLs to reduce fractional spurs. The requantizers are demonstrated and compared to conventional delta-sigma modulators in a low-noise 3.35 GHz PLL IC and shown to offer significant reductions in worst-case spurious tones with similar phase noise relative to their delta-sigma modulator counterparts.

11:45 am      **A 45-75MHz 197-452 $\mu$  W Oscillator with 164.6dB FoM and 2.3ps<sub>rms</sub> Period Jitter in 65nm CMOS**, J. Zhu, M. Mahalley\*, G. Shu, W.-S. Choi, R.K. Nandwana, A. Elkholy, B. Sahoo, P.K. Hanumolu, University of Illinois at Urbana Champaign, \*Analog Devices  
3-5

This paper presents a novel oscillator architecture that uses a low frequency temperature stable clock generated by a low power RC relaxation oscillator to improve the temperature stability of a low noise ring oscillator. Fabricated in 65nm CMOS process, the prototype oscillator consumes 197 to 452 W across an output frequency range of 45-to-75MHz. At

70MHz, the measured period jitter is 2.3psrms with phase noise of -104dBc/Hz at 100kHz offset, which translates to an FoM of 164.6dB.

### Session 4 - Modeling and Measurement of Mixed-Signal Circuits

Monday, May 1, 10:00 - 12:00, Lady Bird 3 Room  
Session Chair: Colin McAndrew, NXP Semiconductors  
Session Co-Chair: Tetsuya Iizuka, University of Tokyo

This session presents a completely generic formalism for modeling devices with internal states, a new approach to design centering, and methodologies for ADC measurement.

10:00 am      **Introduction**

10:05 am      **Modelling Multistability and Hysteresis in ESD Clamps, Memristors and other**  
4-1              **Devices (Invited)**, Tianshi Wang, University of California, Berkeley

Multistability and hysteresis are widely occurring phenomena in devices, leading to many misconceptions among compact model developers. In this paper, we show how hysteretic devices can be modelled in general using only continuous/smooth primitives in a differential equation format suitable for simulation, and how the models can be implemented properly in languages like Verilog-A and ModSpec (MATLAB). Apart from a general model template, several concrete device examples are described and analyzed, including a new compact model for ESD protection devices, new memristor models, a simplified electro-thermal model for HBTs, and a modified Stoner-Wohlfarth model for ferromagnets. Common features of these models are studied to further illustrate the modelling methodology for multistability and hysteresis in devices.

10:55 am      **A Yield Optimization Methodology for Mixed-Signal Circuits**, A. Papadopoulou, B.  
4-2              Nikolic, University of California at Berkeley

With technology scaling in the nanometer regime relative variability increases and becomes more complex, making traditional statistical modeling insufficient. To optimize yield, circuit designers need to determine effects of variations on particular circuit designs, which requires statistical modeling. This paper presents a methodology for simple, fast, design-specific yield optimization that is accessible to the circuit designer. The methodology utilizes backward propagation and convex optimization techniques to customize existing statistical model cards to a given design. The methodology is verified using comparator offset measurements on a 28nm FDSOI technology. The customized model achieves a mean absolute percentage error of < 4% compared to a 30% error in the original models.

11:20 am      **Measurement of High-Speed ADCs (Invited)**, L. Kull\*, D. Luu\*\*, IBM Research -  
4-3              Zurich, \*\*ETH Zurich

High-speed ADCs are challenging in design and measurement. Accuracy on data and clock input are of high importance and are discussed and a test-setup described. An efficient shift-register based approach for an on-chip memory to handle the large aggregated output data of highly interleaved ADCs is presented and discussed in detail.

### Session 5 - Memory for Emerging Applications

Monday, May 1, 10:00 - 12:00, Lady Bird Studio Room  
Session Chair: Muhammad Khellah, Intel  
Session Co-Chair: Rajiv Joshi, IBM

This session presents a 64Mb ReRAM with reliable RD/WR operations, offset-cancelling sense-amplifier for ReRAM, value-aware vertical 3D TLC NAND flash memory, and adaptive circuit assists for enabling SRAM operation at NTV.

10:00 am      **Introduction**

10:05 am      **A 0.13 $\mu$ m 64Mb HfOx ReRAM Using Configurable Ramped Voltage Write and Low Read-Disturb Sensing Techniques for Reliability Improvement**, Xiaowei Han<sup>1</sup>, Qian Jia<sup>1</sup>, Hongbin Sun<sup>2</sup>, Longfei Wang<sup>2</sup>, Huaqiang Wu<sup>3</sup>, Yimao Cai<sup>4</sup>, Feng Zhang<sup>5</sup>, Yongyi Xie<sup>1</sup>, Fangxu Dong<sup>1</sup>, Xiaoguang Wang<sup>1</sup>, Xiaofei Xue<sup>1</sup>, Li Pang<sup>1</sup>, Xiaoqing Zhao<sup>2</sup>, Mengnan Wu<sup>2</sup>, Pu Bai<sup>2</sup>, Qi Liu<sup>5</sup>, Hangbing Lv<sup>5</sup>, Bing Yu<sup>1</sup>, Chao Zhao<sup>5</sup>, He Qian<sup>3</sup>, Ru Huang<sup>4</sup>, Ming Liu<sup>5</sup>, Yumei Zhou<sup>5</sup>, Nanning Zheng<sup>2</sup> and Qiwei Ren<sup>1</sup>. <sup>1</sup>Xi'an UnilC Semiconductors Co., Ltd., <sup>2</sup>Xi'an Jiaotong University, <sup>3</sup>Tsinghua University, <sup>4</sup>Peking University, <sup>5</sup>Chinese Academy Sciences

This paper presents a 0.13 $\mu$ m 64Mb HfOx ReRAM for embedded storage in IoT device. The configurable ramped voltage write and low read-disturb sensing techniques are proposed to address the reliability challenges in ReRAM. Experimental results show that, the ReRAM chip achieves more than 10<sup>7</sup> cycles' endurance and 10 years' retention at 75°C. In addition, its full function and superior random write performance are demonstrated on a developed evaluation board.

10:30 am      **Programmable Supply Boosting Techniques for Near Threshold and Wide Operating Voltage SRAM**, R. V. Joshi, M. M. Ziegler, IBM  
5-2

This paper explores techniques allowing low voltage SRAM operation appropriate for emerging hardware paradigms, such as, IoT and deep learning accelerators. We present new programmable enhancements for voltage supply boosting and a new 14nm test chip for further reducing V<sub>min</sub> as well as operation across a wide voltage range.

10:55 am      **12x Bit-Error Acceptable, 300x Extended Data-Retention Time, Value-Aware SSD with Vertical 3D-TLC NAND Flash Memories for Image Recognition**, Y. Deguchi, T. Nakamura, A. Kobayashi, K. Takeuchi, Chuo University  
5-3

Value-Aware SSD with Vertical 3D-TLC (Triple-Level Cell) NAND flash for the image recognition is proposed to increase the acceptable bit-error rate (BER) by 12-times, extend the data-retention time by 300-times, and decrease the read time by 26%. The proposed SSD combines new data-aware techniques with deep neural network's error tolerance.

11:20 am      **A 256kb 6T Self-Tuning SRAM with Extended 0.38V-1.2V Operating Range using Multiple Read/Write Assists and VMIN Tracking Canary Sensors**, A Banerjee, Ningxi Liu, H. N. Patel, B. H. Calhoun, J. Poulton\*, C. T. Gray\*, University of Virginia, \*Nvidia Corporation.  
5-4

A closed-loop self-tuning 256kb 6T-SRAM with 0.38V-1.2V extended operating range using combined read and write assists and canary-based VMIN-tracking is presented. A 337X and 4.3X power reduction are achieved using multiple assists and VMIN-tracking respectively and combining both saves 1444X in active power and 12.4X in leakage at the 0.38V.

11:45 am  
5-5

**An Offset-Cancelling Four-Phase Voltage Sense Amplifier for Resistive Memories in 14nm CMOS**, A. Biswas, U. Arslan\*\*, F. Hamzaoglu\*\* and A. P. Chandrakasan, Massachusetts Institute of Technology, \* Intel Corporation

This paper presents a low-offset read sensing scheme for resistive memories. In this work we propose a full offset cancellation technique of the sense-amplifier, making it more suitable to tolerate variation from the memory array due to storage device resistance variation.

**Session 6 - RF and Millimeter-Wave Power Amplifiers and Transmitters**

Monday, May 1, 1:30 - 3:00, Lady Bird 1 Room  
Session Chair: Alireza Shirvani, Invensense  
Session Co-Chair: K. J. Koh, Virginia Institute of Technology

This session covers various aspects of efficient signal up-conversion, amplification, and amplifier linearization at RF and millimeter-wave frequencies.

1:30 pm      **Introduction**

1:35 pm      **Millimeter-Wave Power Amplifiers & Transmitters (Invited)**, H. Hashemi, University  
6-1              of Southern California

This review paper covers the basic principles, architectures, and representative results related to millimeter-wave silicon power amplifiers and transmitters.

2:25 pm      **A 3-7GHz 4-Element Digital Modulated Polar Phased-Array Transmitter with 0.35°  
6-2              Phase Resolution and 38.2% Peak System Efficiency**, H. J. Qian<sup>1,2</sup>, J. O. Liang<sup>2</sup>, N. Zhu<sup>2</sup>, P. Gao<sup>2</sup>, X. Luo<sup>1,2</sup>, <sup>1</sup>UESTC, <sup>2</sup>Huawei Technologies Co., Ltd

A 3-7GHz 4-element digital modulated polar phased-array TX in 40nm CMOS with 0.35° phase resolution and 38.2% peak system efficiency is presented. PM phase-shifting is proposed for power saving and better amplitude error. The RMS phase error of 0.3° is achieved with current-DAC based 10-bit phase shifter after digital pre-distortion.

2:50 pm      **Linearization of Multiphase SCPAs (Invited)**, A. Azam, Z. Bai, A. Saha, W. Yuan, J. S.  
6-3              Walling, University of Utah

In this paper, we introduce the multiphase switched-capacitor power amplifier (MP-SCPA). The MP-SCPA is a digital power amplifier (DPA) that achieves a linear output response using a vector summation of two amplitude weighted constant phase signals. In this way, it avoids using a wideband phase modulator that is required in other DPAs. The MP-SCPA is subject to non-linearity induced by bondwires and other packaging associated inductance that causes variation in the voltage supply available on-chip. To correct for this packaging based non-linearity, we propose a polar digital pre-distortion that is more robust and requires less chip area than traditional lookup table based methods. A prototype MP-SCPA is measured with the polar DPD and found to have similar performance when compared with a dense lookup table based DPD. The MP-SCPA is measured with a 5 MHz, 64 QAM LTE signal and achieves a measured ACLR < -30 dBc, an EVM=3.4%-rms and an average system efficiency of 15.8%.

3:15 pm **Break**

**Session 7 - Data Converter Techniques**

Monday, May 1, 1:30 - 5:30, Lady Bird 2 Room  
Session Chair: Ayman Shabra, MediaTek  
Session Co-Chair: Dong-Young Chang, Maxim

Broad range of oversampling converters ranging from application specific to structural innovations are presented in this session.

1:30 pm **Introduction**

1:35 pm **A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration**, Yeonam Yoon, Nan Sun, University of Texas at Austin  
7-1

This paper presents a 6-b high-speed SAR ADC with sparkle code correction. By quantizing the comparator decision time, sparkle codes are corrected. Furthermore, CDT quantization enables 1-bit increase in ADC resolution. A novel dither-based background calibration technique is devised to accurately control the CDT detection window and ensure PVT robustness.

2:00 pm **A Pipelined SAR ADC Reusing the Comparator as Residue Amplifier**, M. Gandara, W. Guo, X. Tang, L. Chen, Y. Yoon, N. Sun, University of Texas-Austin  
7-2

This paper presents a 12-bit pipelined SAR ADC that reuses the comparator from the first-stage SAR to perform residue amplification. The proposed amplifier utilizes positive feedback to achieve a large gain at high speed. To the authors' knowledge, this work achieves the highest interstage gain of any reported dynamic amplifier.

2:25 pm **A 74.33 dB SNDR 20 MSPS 2.74 mW Pipelined ADC using a Dynamic Deadzone Ring Amplifier**, S. Leuenberger, J. Muhlestein, H. Sun, P. Venkatachala, U. Moon, Oregon State University  
7-3

This work is a ring amplifier built with current-starved inverters in the intermediate stage. This structure combined with a dynamic deadzone combines the properties of both coarse estimation and fine settling. The ADC consumes 2.74 mW and achieves a peak SNDR of 74.33 dB which provides a FoM of 32.2 fJ/c-step.

2:50 pm **A 12-/14-bit, 4/2MSPS, 0.085mm<sup>2</sup> SAR ADC in 65nm Using Novel Residue Boosting**, Joonsung Park, Krishnaswamy Nagaraj, Mikel Ash\*, Ajay Kumar\*\*, Texas Instruments, \*Cirrus Logic, \*\*Microchip  
7-4

In this paper, a re-configurable 12/13/14-bit SAR ADC based on a 12-bit ADC core is presented. A novel residue-boosting algorithm is developed to increase the bit resolution of a SAR ADC up to 2 bits without significant additional area and power. In the 12-bit mode, the 65nm prototype shows both DNL and INL of about +/- 0.5 LSB at 4MSPS, and in 14-bit mode, DNL and INL are about +/- 1 LSB and +/- 2 LSB at 2MSPS. ENOB is 11.5 bit and 13 bit for 12-bit and 14-bit mode each. The area of the ADC is 0.085mm<sup>2</sup>.

3:15 pm **Break**

3:30 pm  
7-5 **A Background Calibrated 28GS/s 8b Interleaved SAR ADC in 28nm CMOS**, Michael Q. Le, James Gorecki, Jamal Riani, Jorge Pernillo, Amber Tan, Karthik Gopalakrishnan, Belal Helal, Pulkit Khandelwal, ChangFeng Loi, Irene Quek, Pui Wong, A. Buchwald, Inphi Corp.

A 28-GS/s time-interleaved ADC suitable for PAM4 optical and backplane applications is presented. The architecture uses a two-rank 2x(4:4) sampling network to interleave 32 8b SAR ADCs employing redundancy to relax DAC settling requirements. A DSP core estimates and corrects the gain, offset and timing error between channels. An ENOB of 5.8b and 5.4b is achieved with 1-GHz and 13.3GHz input signals. The ADC consumes 165-mW from a single 950-mV power supply and is fabricated in a 28nm CMOS process occupying 0.24mm<sup>2</sup>.

3:55 pm  
7-6 **A 10-b 2b/cycle 300MS/s SAR ADC with a Single Differential DAC in 40nm CMOS**, J. Song, X. Tang, N. Sun, University of Texas at Austin

This paper presents a 300MS/s single-channel 2b/cycle hybrid SAR with only 1 differential DAC. The proposed architecture exploits both differential and common mode voltages to generate 3 comparison levels needed for 2b/cycle without requiring extra DAC. It achieves peak 8.5b ENOB and consumes 2.1mW. FoM of 19.3fJ/conv-step is achieved.

4:20 pm  
7-7 **A 73dB SNDR 20MS/s 1.28mW SAR-TDC Using Hybrid Two-Step Quantization**, J. Muhlestein, S. Leuenberger, H. Sun, Y. Xu, U. Moon, Oregon State University

A Hybrid SAR-TDC technique offers scalability, simplicity and efficiency. Quantization is performed on both voltage and time domain signals. Measured prototype demonstrates an SNDR of 73 dB at 20 MSPS and 1.28 mW power for a Walden Figure of merit of 17.4 fJ/conversion-step.

### Session 8 - Biomedical Circuits and Systems

Monday, May 1, 1:30 - 5:30, Lady Bird 3 Room  
Session Chair: Pedram Mohseni, Case Western Reserve University  
Session Co-Chair: Kaushik Sengupta, Princeton University

The session focuses on biomedical applications of integrated circuits and systems ranging from power delivery to implantables, to physiological signal monitoring and cell-level sensing.

1:30 pm **Introduction**

1:35 pm  
8-1 **Design of Miniaturized Wireless Power Receiver for mm-sized Implants (Invited)**, Chul Kim, Sohmyung Ha\*, Abraham Akinin, Jiwoong Park, Rajkumar Kubendran, Hui Wang, Patrick P. Mercier, Gert Cauwenberghs, University of California, San Diego, \*New York University Abu Dhabi

Current WPT technique relies on bulky power receiving (RX) coil and power storage decoupling capacitors, disturbing the realization of mm-sized implants. Ultimate miniaturization is possible by integrating such external bulky components into on-chip wireless power receivers. In this paper, two fully integrated wireless power receiver for mm-sized implants are introduced.

2:00 pm  
8-2 **A Power-Efficient Multi-Channel PPG ASIC with 112dB Receiver DR for Pulse Oximetry and NIRS**, P. Schönle, S. Fateh, T. Burger, Q. Huang, ETH Zurich



The chip supports probes with up to 32 LEDs and 4 photodiodes and features a receiver that covers a wide input current range. A higher power-efficiency than the state-of-the-art results in 68% less total power consumption (incl. LEDs) for equal performance or 7dB higher performance at equal power consumption.

2:25 pm  
8-3

**A Dynamically Reconfigurable ECG Analog Front-End with a 2.5× Data-Dependent Power Reduction**, Somok Mondal, Chung-Lun Hsu, Roozbeh Jafari\*, Drew Hall, University of California, San Diego, \*Texas A&M University

An analog front-end (AFE) with agile, on-the-fly noise-power reconfiguration for data-dependent power savings of 2.5× is presented. Implemented in 65nm CMOS the AFE offers programmable noise from 1.90-2.91  $\mu\text{Vrms}$  while consuming 307-769 nW power and is assisted by an LMS-based adaptive linear predictive filter to exploit low-activity and quasi-periodicity of bio-signals.

2:50 pm  
8-4

**CMOS Sensor for Dual Fluorescence Intensity and Lifetime Sensing Using Multicycle Charge Modulation**, Guoqing Fu, Sameer Sonkusale, Tufts University

A novel CMOS sensor chip is proposed to realize both fast and accurate intensity and lifetime sensing for fluorescence. CTIA-based multi-cycle charge modulation achieves 4.38nW/cm<sup>2</sup> resolution for intensity measurement and 45ns resolution for lifetime measurement. Dissolved oxygen is measured with 7.5%/ppm and 6%/ppm sensitivity in both intensity and lifetime domain.

3:15 pm **Break**

3:30 pm  
8-5

**A 255nW Ultra-High Input Impedance Analog Front-End for Non-contact ECG Monitoring**, Jinseok Lee, Hyojun Kim, SeongHwan Cho, KAIST

In this paper, we propose a high input impedance analog front-end for low-power biopotential acquisition. All of parasitic capacitance including off-chip, PAD, ESD, and transistor gate at the input were cancelled using positive feedback. A prototype IC fabricated in 0.18 $\mu\text{m}$  CMOS consumes 255nW and has input capacitance of 60fF.

3:55 pm  
8-6

**A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for Forward-Looking Intravascular Ultrasound**, Mingliang Tan, Chao Chen, Zhao Chen, Jovana Janjic\*, Verva Daeichin\*, Zu-yao Chang, Emile Noothout, Gijs van Soest\*, Martin Verweij, Nico de Jong, and Michiel Pertijs, Delft University of Technology, \*Erasmus MC

This paper presents a front-end ASIC for forward-looking intravascular ultrasound imaging. It is intended to be mounted at the tip of a catheter and interfaces 80 piezo-electric transducer elements with an imaging system using only 4 cables, thus significantly reducing the system complexity compared to the prior art.

4:20 pm  
8-7

**Interference-immune Diagnostic Quality ECG Recording for Patient Monitoring Applications**, A. Kalb, Y. Sharma, Analog Devices Inc.

This paper describes an ECG conversion channel providing diagnostic quality readouts while under severe interference. The input dynamic range is greater than  $\pm 1$  V with an overload recovery time of approximately 12 ms. Input bias currents are maintained below 150 pA. The noise per channel is approximately 1.2  $\mu\text{Vrms}$ .

4:45 pm  
8-8

**A CMOS 22k-Pixel Single-Cell Resolution Multi-Modality Real-Time Cellular Sensing Array**, J. Park, M. Aziz, S. Gonzalez\*, D. Jung, T. Chi, S. Li, H. Cho\*, H. Wang, Georgia Institute of Technology, \*Emory University

This paper presents a 22k-pixel multimodality sensing array with a DCCA for cell characterization and drug screening. DCCA achieves the measured input-referred noise of  $2.46\mu\text{Vrms}$  and cell-based measurements successfully capture the beating rate of cardiomyocytes using both optical detection and potential recording. Additionally, drug effects of isoproterenol are successfully characterized.

**Session 9 - Panel - Hardware and Software  
Security: Gaps and Synergies**

Monday, May 1, 1:30 - 5:30, Lady Bird Studio Room

Panel Chairs: Nima Maghari, University of Florida and Swaroop Ghosh, University of South Florida

**Panelists:**

Ram Krishnamurthy, Intel

Arnett Brown, Booz Allen Hamilton

Patrick Schaumont, Virginia Tech

Kanad Ghose, Binghamton University

Trent Jaeger, Pennsylvania State University

This panel will review the fundamental software and hardware security issues and state-of-the-art solutions proposed by academia and industry. The panel will also identify the synergies and gaps between software and hardware security to benefit the researchers from both communities.

**Session 10 - Forum - Technology, Circuits and  
Systems for 5G Communication**

Monday, May 1, 3:30 - 5:30, Lady Bird 1 Room

Forum Chairs : John Long, University of Waterloo and Hua Wang, Georgia Institute of Technology

The aim of this forum is to bring the fifth-generation of mobile communications into sharper focus as it nears commercialization. Recent developments in 5G-communications technology and standards are examined in detail by the 5 speakers in the forum. The presentations range from IC technology (process options for mm-wave radio development on silicon), to circuits for practical wideband radios, systems-level considerations (higher transceiver efficiency), and consequences of recent standardization efforts on design and IC implementation.

1:30 pm      **Introduction**

1:35 pm      **3GPP 5G Standardization Status; RF and mm-Wave Challenges of New Radio,**  
10-1          Dominique Brunel, Skyworks Inc

The status of on-going 5G New Radio, 3GPP standardization work will be covered for both traditional frequencies below 6GHz and new spectrum in the cm/mm-wave region. New 3GPP NR features enabling multiple numerology, lower latency and antenna beamforming are described together with new waveforms, coding and modulations schemes that have been introduced. Finally, implications of these new techniques to signal processing, analog and RF blocks will be analyzed and associated RF and mm-wave technology and design challenges will be discussed, focusing on the impact on RF front-end and RFIC technology.

2:10 pm      **5G Standards Progress and Challenges,** Takao Inoue, National Instruments

10-2

The 3GPP standardization process for 5G has been in full gear since early 2016. In this talk, we review some of the key technical areas that could impact future designs, e.g., waveforms, numerology, multi-antenna, and mm-wave technologies, and discuss challenges associated with them.

2:45 pm  
10-3

**5G Signals and Power Amplifier Energy Efficiency**, Earl McCune, Eridan Communications

The present signal proposals under consideration for 5G standardization are all challenging to RF power amplifier designers. Particularly for massive-MIMO arrays, the energy efficiency challenge is critical for achieving practical array operating temperatures. This presentation examines how the present panoply of PA architectures can address these challenges, with examples.

3:20 pm

**Break**

3:35 pm  
10-4

**Practical 5G mm-Wave Solutions**, Jonathan Jensen, Intel Corp

This presentation will describe a prototype and potential circuits and hardware for 5G solutions. The impact of 5G requirements on circuits and systems will be outlined; along with examples from 5G mm-wave demonstration vehicles.

4:10 pm  
10-5

**Process Options and mm-Wave Reference Circuits for 5G Communication**,  
Chaojiang Li, Global Foundries Inc.

Integrated circuit technologies suitable for 5G front-end module (FEM) applications are described in this presentation. To implement the FEMs, we will introduce GF 45-nm RFSOI: FETs, the substrate, back end-of-line options, and mm-wave characterizations to show its advantages. A 22-nm technology (GF 22FDX) aimed at highly-integrated transceivers that is optimized for low-power, high digital density capability, and also excellent mm-wave performance is also described. GF internal and published examples of switch, PA, and LNA design benchmarks in these technologies will also be presented.