**Educational Sessions**
**Sunday, April 30**

## Educational Session 1: Mm-Wave/RF Wireless

**Room:** Lady Bird 1
**Chair:** Yanjie Wang, Intel
**Co-Chair:** Foster Dai, Auburn University

**ES1-1**
8:30 - 10:00 am
**Mm-wave LO Distribution Insights,** Amr Fahim, Inphi Corporation
Recent technology advances have enabled millimeter wave (mmWave) transceiver technology to be integrated into silicon in a cost-effective manner. One main challenge in enabling millimeter wave circuitry is local oscillator (LO), or clock signal, distribution throughout the millimeter wave transceivers. In this talk, recent advances and techniques in LO distribution are discussed. State-of-the-art circuit techniques and topologies enabling trade-offs between skew, duty cycle, power consumption and phase noise in mmWave LO distribution is discussed in detail. Special case study of a phased-array system is used to demonstrate such techniques.

**ES1-2**
10:30 - 12:00 pm
**On-chip transformer design and application to RF and mm-wave front-ends,** John Long, University of Waterloo
Monolithic transformers have been applied to RF applications such as: VCO resonators, low-loss feedback networks, baluns, power combiners/splitters, and even ESD protection networks for wideband inputs. The design of transformers for RF, and in particular mm-wave, applications is covered in this short course. Transformer design for a specific bandwidth, insertion loss and transformation ratio is outlined. Methods for shielding, which is essential to reduce substrate losses in on-chip transformers at mm-wave frequencies are also described. Modeling for simulation (both small- and large-signal) of circuits in a typical design flow is also presented. Application-specific aspects of transformer design for VCOs, LNAs, mixers, and power amplifiers are detailed throughout the presentation using mm-wave case studies as design examples.

**ES1-3**
1:00 - 2:30 pm
**Doherty Architecture For mm-wave/RF Digital and Analog Power Amplifiers,** Hua Wang, Georgia Institute of Technology
Doherty architecture is recently gaining an increasing interest due to its back-off region (PBO) efficiency enhancement and its compatibility with broadband and linear amplifications. This short course will first introduce the Doherty PA and its operation principle. Multiple popular architectures will be presented, and their pros and cons will be discussed. Several recently published PAs using standard CMOS/SiGe processes will be shown as designs examples to demonstrate the use of Doherty architecture in low-GHz mixed-signal power amplifiers and mm-Wave 5G multi-band analog power amplifiers.

**ES1-4**
3:00 - 4:30 pm
**Wireless Transmitter Measurement Techniques - Equalization, Algorithms, Trade-off Analysis,** Srevats Laxman, Tektronix,
With 5G, lots of research is taking place in the millimeter wave spectrum. Some of the challenges for this spectrum are how to model the channel and how the receiver will be able to recover the transmitted data effectively. Equalization is the mechanism used in receiver to account for the distortion caused by the channel and is one of the important blocks of a demodulator design along with Symbol and Carrier recovery. Equalization is critical for important measurements such as Error Vector Magnitude. In this presentation we will discuss techniques used in Equalizers for standards that operate in Millimeter wave range.

## Educational Session 2: Analog and Frequency Synthesis

**Room:** Lady Bird 2
**Chair:** Axel Thomsen, Cirrus Logic
**Co-Chair:** Ion Tesu, Silicon Labs

**ES2-1**
8:30 - 10:00 am
**Achieving Higher Linearity in Precision Standard Products,** Nathan Carter, ADI
A review of the linearity performance of close loop standard products will be presented with an emphasis on achieving the best loop bandwidth given a limited power budget.

**ES2-2**
10:30 - 12:00 pm
**Active Filters: Design Methods & Trade-offs of New Approaches,** Edgar Sanchez-Sinencio, Texas A&M University
Electronic filters is a familiar topic for analog designers. We will briefly discuss their origin and its evolution. From passive discrete components filter, active-RC with tubes (bulbs), then with transistors and finally monolithic and fully integrated. The integrated CMOS Active –RC has morphed into very creative and practical filters. In particular, we will touch key issues of the following filter types: Active-R, Switched-R, Ring Oscillator Based, PWM Based.

**ES2-3**
1:00 - 2:30 pm
**Area Efficient Sub-Sampling PLL Synthesizer with Robust Locking,** Foster Dai, Auburn University
Modern RF frequency synthesizer designs are driven by ever increasing system requirements such as low power, low phase noise and multi-phase clock generations. Traditional LC based PLLs occupy large area and present challenges for technology scaling. On the other hand, area efficient ring oscillators (ROs) often suffer from poor jitter and phase noise performances. Recent techniques including injection locking (IL) and sub-sampling (SS) have achieved impressive in-band noise performance. As a result, the integrated phase noise of inductorless PLLs can be greatly improved with a widened loop bandwidth. Improving spectral purity is normally obtained at the price of higher power consumption. This talk discusses the techniques to break this trade-off by both circuit and architectural innovations. This talk addresses the design challenges such as the stability issues associated with SSPLLs and the reference spur issues introduced in ILPLLs.

**ES2-4**
3:00 - 4:30 pm
**Practical Dynamic element matching techniques for 3-level unit elements,** Khiem Nguyen, ADI
The presentation gives an overview of 3-level unit element usage in multi-bit oversampling data converter designs and the analysis of 3-level mismatch shaping, and in particular what mismatch shaping will and will not solve in those applications. Design and analysis of several practical $1^{st}$-order DEM algorithms such as DWA, rotational schemes, issues and remedies associated with these schemes will be discussed. A generalized model of 3-level DEM will then be presented and how this model leads to an efficient $2^{nd}$-order DEM algorithm. Examples of these designs in silicon will be shown to help the audience visualize the usage of 3-level DEM in high precision data converter applications. Concept such as variable length DEM targeted for low power design will be discussed, followed by a conclusion and suggested areas for future works.

## Educational Session 3: Advanced Technologies and Diversity

**Room:** Lady Bird 3
**Chair:** Jiangfeng Wu, Tongji University
**Co-Chair:** Mike Mulligan, Silicon Labs

**ES3-1**
8:30 - 10:00 am
**Energy Efficient System Architecture for Wireless Wearable Biomedical Sensors,** Lian Yong, York University,
This tutorial will cover several topics related to challenges in the design of low power wearable wireless biomedical sensor chip including regulatory requirements, skin-electrode interface, design considerations of analog frontend, ADC, signal processing, and wireless transceiver. The focus is on the energy efficient system architecture for wearable wireless biomedical sensor SoC. Design example, such as self-powered wearable ECG sensor, will be discussed in detail.

**ES3-2**
10:30 - 12:00 pm
**Leveraging the Strengths of Female Engineers in Today's Business Environment,** Susanne Paul, Qualcomm,
Differences between the brains of men and women result in different engineering styles. These styles complement one another and are powerful when combined. Women would achieve greater success for themselves and their teams if the engineering community recognized the value of and better leveraged female engineering styles.

**ES3-3**
1:00 - 2:30 pm
**Design with sub-10 nm FinFET technologies,** Larry Clark, Arizona State
This educational session will describe the impact of FinFET and multi-patterning on design choices in logic and memory. Transistor structure as well as middle-of-line layers and their impact on design at the 7-nm and 5-nm generations, as well as the Differences between the brains of men and women result in different engineering styles. These styles complement one another and are powerful when combined. Women would achieve greater success for themselves and their teams if the engineering community recognized the value of and better leveraged female engineering styles. Impact of EUV on layout are discussed. Design/technology co-optimization will be reviewed, illustrating the impact of constrained structures (layout choices) on the designer's choices. Standard cell, SRAM, and digital block electrical and physical design will be used as examples. The aim is to provide designers not only with what to expect in these generations, but insights into the process and device architecture impact on design rules and design constraints.

**ES3-4**
3:00 - 4:30 pm
**RF/Analog and Mixed-Signal Design Techniques in FD-SOI Technology,** Andreia Cathelin, ST Microelectronics
Fully Depleted Silicon on Insulator (FD-SOI) is one of the alternatives that permits today to follow the More Moore law of CMOS integration for the 28nm node and beyond, while still dealing with fully planar transistors. Numerous presentations have highlighted over last years the benefits of this technology for an energy efficient integration of digital signal processing cores. This short course presentation will focus on the benefits of FD-SOI technology for analog/RF/millimeter-wave and high-speed mixed signal circuits, by taking full advantage of wide voltage range body biasing tuning. For each category of circuits (analog/RF, mmW and high-speed), concrete design examples are given in order to highlight the main design features specific to FD-SOI and the resulting performances.

## Education Session 4: Data and Power Converter

**Room:** Lady Bird Studio
**Chair:** Nan Sun, Univ. of Texas, Austin
**Co-Chair:** Mark Ren, Nvidia

**ES4-1**
8:30 - 10:00 am
**Time Based $\Delta\sum$-ADC Design Techniques,** Pavan Kumar Hanumolu, University of Illinois Urbana-Champaign
Oversampling analog to digital converters are commonly implemented in voltage, current, or charge domains. High precision is typically achieved by processing voltage/current/charge using high gain amplifiers embedded in negative feedback. However, achieving high gain in deeply scaled and beyond CMOS technologies is difficult. In this talk, I will discuss how to implement high precision analog to digital converters using time-based signal processing. I will describe how this alternate signal representation allows use of simple CMOS ring oscillators (RO) to perform high precision conversion. After highlighting the main advantages of RO-based ADCs, I will describe their drawbacks and present techniques to overcome them. I will present several case studies of high performance ADCs that utilize these techniques to achieve state-of-the-art performance.

**ES4-2**
10:30 - 12:00 pm
**A/D Converter Fundamentals and Trends,** Hui Pan, Broadcom
This tutorial aims to lower the barrier to entry for newcomers, while providing new angles for incumbent practitioners by deriving the ADC fundamentals and trends in a logical and unified framework. The course opens with a survey of the latest developments in ADC applications and a brief theory on sampling and quantization, followed by a systematic derivation of quantizer architectures from search algorithms. Basic circuit building blocks, their imperfections, remedies, and characterizations are then highlighted. The course concludes with examples of ADC design evolutions to further illustrate the key points

**ES4-3**
1:00 - 2:30 pm
**DC-DC Power Converter Designs,** Ramesh Harjani, University of Minnesota
This tutorial aims to discuss the overview and recent trend of DC-DC converters architectures and circuit implement.

**ES4-4**
3:00 - 4:30 pm
**Circuit Design Techniques for Fully Integrated Voltage Regulator Using Switched Capacitors,** Hanh-Phuc Le, University of Colorado
In this talk, the speaker will focus on switched-capacitor as a good candidate for the solution. The speaker will first briefly discuss the needs and trade-offs between different types of converters to motivate the use of fully integrated switched capacitor DC-DC converter. The main part of the talk will cover circuit techniques in designing this type of converter in order to improve its power density, efficiency, transient response and input/output voltage range. Design examples in literature will be given in accordance with these design techniques. At the end of the talk, the speaker will also discuss other current and future applications that could lead to a major change in DC power delivery industry.