CICC Technical Program

Session 1 - Plenary
Monday, May 1, 8:00 - 9:30, Lady Bird 1 Ballroom

1 **Autonomy with Smart Power Electronics**, Hans Stork, ON Semiconductor

Session 2 - Wireline Techniques forAdvanced Modulation Schemes
Monday, May 1, 10:00 - 12:00, Lady Bird 1 Room
Session Chair: Sudip Shekhar, University of British Columbia
Session Co-Chair: Tod Dickson, IBM

2-1 **A Supposedly Clever Thing I'll Never Do Again**, Aaron Buchwald, Inphi

This paper will review a few "clever" ideas with disappointing results, focusing primarily the use of a slow, but accurate, reference ADC for system-identification approaches to background calibration in time-interleaved ADCs, where complications ultimately limit performance in a variety of unanticipated ways.

2-2 **Channel Adaptive ADC and TDC for 28 Gb/s 4pJ/bit PAM-4 Digital receiver**, Aurangozeb, AKM Delwar Hossain, Masum Hossain, University of Alberta

A low power channel adaptive 28 Gb/s PAM-4 receiver utilizes a predictive 2-to-5.5-bit ADC, a 5-bit SAR TDC, and a 3-to-8 programmable tap FFE in digital domain. Measured power consumption is 130mW(excluding DSP). The receiver enables energy proportional loss compensation with average energy efficiency better than 4 pJ/bit including DSP.

2-3 **A 4-40 Gb/s PAM4 Transmitter with Output Linearity Optimization in 65 nm CMOS**, Xuqiang Zheng, Chun Zhang , Fangxu Lv , Feng Zhao*, Shigang Yue*, Ziqiang Wang , Fule Li , Hanjun Jiang , and Zhihua Wang , Tsinghua University, *University of Lincoln

This paper presents a 4-40Gb/s current mode PAM4 transmitter in 65nm CMOS. By embedding current-compensating circuits into the output driver and developing a coherent scaled-replica based bias generator, the peak-to-peak swing achieves 960mV with an eye linearity of 1.01 in AC coupling mode.

2-4 **A 10-to-650MHz 1.35W Class-AB Power Amplifier with Instantaneous Supply-Switching Efficiency Enhancement**, J. Lee, S. Pamarti, R. Gomez*, UCLA, *Broadcom Ltd.

A novel PA supply-modulation technique is introduced. Cascode transistors switch output signal current to high/low supply rails depending on instantaneous amplitude. GHz-rate current-mode switching enhances efficiency for bandwidths beyond existing envelope trackers. 1.35W peak power and efficiency=13.6%@11dB PAPR are observed. Combined Pout, fractional bandwidth and high-PAPR efficiency exceed prior art.

Session 3 - Clocking Techniques
Monday, May 1, 10:00 - 12:00, Lady Bird 2 Room
Session Chair: Sudhakar Pamarti, UCLA
Session Co-Chair: Nan Sun, University of Texas

3-1 **A 0.951 psrms Period Jitter, 3.2% Modulation Range, DSM-Free, Spread-Spectrum PLL**, H. Sun, K. Sobue*, K. Hamashita*, T. Anand, and U. Moon, Oregon State University, Asahi Kasei Microdevices*.

This work presents a DSM-free spread-spectrum PLL. The proposed charge-based discrete-time loop filter enables wide and PVT-insensitive modulation. Correlated double sampling minimizes noise penalty. This work achieves 3.2% spread-spectrum modulation range with 26.51dB attenuation. Implemented in 0.18µm CMOS, this work achieves 951fsrms period jitter while consuming 9.93mW from 1.8V supply.

3-2 **A 0.031mm2, 910fs, 0.5-4GHz Injection Type SOC PLL with 90dB Built-in Supply Noise Rejection in 10nm FinFET CMOS**, Chin-Yang Wu, Ruei-Pin Shen, Chih-Hsien Chang, Kenny Hsieh, Mark Chen, TSMC

This paper presents a wide operating range (0.5~4GHz) PLL using soft injection techniques. Its ring-type VCO achieves built-in 90dB PSRR. This design achieves 910fs RMS phase jitters and -58dBc/Hz reference spur of a 3GHz output. The prototype PLL is fabricated in 10nm Fin-FET process with an active area of 0.031mm^2.

3-3 **A -236.3dB FoM Sub-Sampling Low-Jitter Supply-Robust Ring-Oscillator PLL for Clocking Applications with Feed-Forward Noise-Cancellation**, Shravan S. Nagam, Peter R. Kinget, Columbia University

A 2-2.8GHz 65nm CMOS ring oscillator PLL occupies an active area of 0.022mm2, consumes 5.86mW and achieves a 633fs RMS jitter at 2.36 GHz and an FOMjitter of -236.3dB. It implements a low-overhead feed-forward phase and supply-noise cancellation scheme by leveraging the noise extraction inherently done by the sub-sampling phase detector. Cancellation reduces the jitter by 1.4x, the phase noise by 10.2dB to -123.5dBc/Hz at a 300KHz offset, and the ring oscillator supply sensitivity by 19.5dB for a 1mVp-p 100KHz supply noise tone.

3-4 **Second and Third-Order Successive Requantizers for Spurious Tone Reduction in Low-Noise Fractional-N PLLs**, E. Familier, I. Galton, University of California, San Diego

This paper presents 2nd- and 3rd-order digital requantizers which can be used as drop-in replacements for digital delta-sigma modulators in analog fractional-N PLLs to reduce fractional spurs. The requantizers are demonstrated and compared to conventional delta-sigma modulators in a low-noise 3.35 GHz PLL IC and shown to offer significant reductions in worst-case spurious tones with similar phase noise relative to their delta-sigma modulator counterparts.

3-5 **A 45-75MHz 197-452u W Oscillator with 164.6dB FoM and 2.3psrms Period Jitter in 65nm CMOS**, J. Zhu, M. Mahalley*, G. Shu, W.-S. Choi, R.K. Nandwana, A. Elkholy, B. Sahoo, P.K. Hanumolu, University of Illinois at Urbana Champaign, *Analog Devices

This paper presents a novel oscillator architecture that uses a low frequency temperature stable clock generated by a low power RC relaxation oscillator to improve the temperature stability of a low noise ring oscillator. Fabricated in 65nm CMOS process, the prototype oscillator consumes 197 to 452 W across an output frequency range of 45-to-75MHz. At 70MHz, the measured period jitter is 2.3psrms with phase noise of -104dBc/Hz at 100kHz offset, which translates to an FoM of 164.6dB.

Session 4 - Modeling and Measurement of Mixed-Signal Circuits
Monday, May 1, 10:00 - 12:00, Lady Bird 3 Room
Session Chair: Colin McAndrew, NXP Semiconductors
Session Co-Chair: Tetsuya Iizuka, University of Tokyo

4-1 **Modelling Multistability and Hysteresis in ESD Clamps, Memristors and other Devices**, Tianshi Wang, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley

Multistability and hysteresis are widely occurring phenomena in devices, leading to many misconceptions among compact model developers. In this paper, we show how hysteretic devices can be modelled in general using only continuous/smooth primitives in a differential equation format suitable for simulation, and how the models can be implemented properly in languages like Verilog-A and ModSpec (MATLAB). Apart from a general model template, several concrete device examples are described and analyzed, including a new compact model for ESD protection devices, new memristor models, a simplified electro-thermal model for HBTs, and a modified Stoner-Wohlfarth model for ferromagnets. Common features of these models are studied to further illustrate the modelling methodology for multistability and hysteresis in devices.

4-2 **A Yield Optimization Methodology for Mixed-Signal Circuits**, A. Papadopoulou, B. Nikolic, University of California at Berkeley

With technology scaling in the nanometer regime relative variability increases and becomes more complex, making traditional statistical modeling insufficient. To optimize yield, circuit designers need to determine effects of variations on particular circuit designs, which requires statistical modeling. This paper presents a methodology for simple, fast, design- specific yield optimization that is accessible to the circuit designer. The methodology utilizes backward propagation and convex optimization techniques to customize existing statistical model cards to a given design. The methodology is verified using comparator offset measurements on a 28nm FDSOI technology. The customized model achieves a mean absolute percentage error of < 4% compared to a 30% error in the original models.

4-3 **Measurement of High-Speed ADCs**, L. Kull*, D. Luu*,**, IBM Research - Zurich, ETH Zurich

High-speed ADCs are challenging in design and measurement. Accuracy on data and clock input are of high importance and are discussed and a test-setup described. An efficient shift-register based approach for an on-chip memory to handle the large aggregated output data of highly interleaved ADCs is presented and discussed in detail.

Session 5 - Memory for Emerging Applications
Monday, May 1, 10:00 - 12:00, Lady Bird Studio Room
Session Chair: Muhammad Khellah, Intel
Session Co-Chair: Rajiv Joshi, IBM

5-1 **A 0.13µm 64Mb HfOx ReRAM Using Configurable Ramped Voltage Write and Low Read-Disturb Sensing Techniques for Reliability Improvement**, Xiaowei Han ,Qian Jia ,Yongyi Xie ,Fangxu Dong ,Xiaoguang Wang ,Xiaofei Xue ,Li Pang ,Bing Yu ,Qiwei Ren, Hongbin Sun*,Longfei Wang*,Xiaoqing Zhao*,Mengnan Wu*,Pu Bai*,Nanning Zheng*,Huaqiang Wu**,He Qian**,Yimao Cai***,Ru Huang***,Feng Zhang****,Qi Liu**

This paper presents a 0.13µm 64Mb HfOx ReRAM for embedded storage in IoT device. The configurable ramped voltage write and low read-disturb sensing techniques are proposed to address the reliability challenges in ReRAM. Experimental results show that, the ReRAM chip achieves more than 107 cycles' endurance and 10 years' retention at 75°C. In addition,its full function and superior random write performance are demonstrated on a developed evaluation board.

5-2 **Programmable Supply Boosting Techniques for Near Threshold and Wide Operating Voltage SRAM**, R. V. Joshi, M. M. Ziegler, IBM

This paper explores techniques allowing low voltage SRAM operation appropriate for emerging hardware paradigms, such as, IoT and deep learning accelerators. We present new programmable enhancements for voltage supply boosting and a new 14nm test chip for further reducing Vmin as well as operation across a wide voltage range.

5-3 **12x Bit-Error Acceptable, 300x Extended Data-Retention Time, Value-Aware SSD with Vertical 3D-TLC NAND Flash Memories for Image Recognition**, Y. Deguchi, T. Nakamura, A. Kobayashi, K. Takeuchi, Chuo University

Value-Aware SSD with Vertical 3D-TLC (Triple-Level Cell) NAND flash for the image recognition is proposed to increase the acceptable bit-error rate (BER) by 12-times, extend the data-retention time by 300-times, and decrease the read time by 26%. The proposed SSD combines new data-aware techniques with deep neural network's error tolerance.

5-4 **A 256kb 6T Self-Tuning SRAM with Extended 0.38V-1.2V Operating Range using Multiple Read/Write Assists and VMIN Tracking Canary Sensors**, A Banerjee*, Ningxi Liu*, H. N. Patel*, J. Poulton**, C. T. Gray**, B. H. Calhoun*, *University of Virginia, **Nvidia Corporation.

A closed-loop self-tuning 256kb 6T-SRAM with 0.38V-1.2V extended operating range using combined read and write assists and canary-based VMIN-tracking is presented. A 337X and 4.3X power reduction are achieved using multiple assists and VMIN-tracking respectively and combining both saves 1444X in active power and 12.4X in leakage at the 0.38V.

5-5 **An Offset-Cancelling Four-Phase Voltage Sense Amplifier for Resistive Memories in 14nm CMOS**, A. Biswas*, U. Arslan**, F. Hamzaoglu** and A. P. Chandrakasan*.
* Massachusetts Institute of Technology(MIT)
** Intel Corporation

This paper presents a low-offset read sensing scheme for resistive memories.In this work we propose a full offset cancellation technique of the sense-amplifier, making it more suitable to tolerate variation from the memory array due to storage device resistance variation.

Session 6 - RF and Millimeter-Wave Power Amplifiers and Transmitters
Monday, May 1, 1:30 - 3:00, Lady Bird 1 Room
Session Chair: Alireza Shirvani, Invensense
Session Co-Chair: KK Koh, Virginia Tech

6-1 **Millimeter-Wave Power Amplifiers & Transmitters**, H. Hashemi, University of Southern California

This review paper covers the basic principles, architectures, and representative results related to millimeter-wave silicon power amplifiers and transmitters.

6-2 **A 3-7GHz 4-Element Digital Modulated Polar Phased-Array Transmitter with 0.35° Phase Resolution and 38.2% Peak System Efficiency**, H. J. Qian*#, J. O. Liang#, N. Zhu#, P. Gao#, X. Luo*#, *UESTC, #Huawei Technologies Co., Ltd

A 3-7GHz 4-element digital modulated polar phased-array TX in 40nm CMOS with 0.35° phase resolution and 38.2% peak system efficiency is presented. PM phase-shifting is

proposed for power saving and better amplitude error. The RMS phase error of 0.3° is achieved with current-DAC based 10-bit phase shifter after digital pre-distortion.

6-3 **Linearization of Multiphase SCPAs**, A. Azam, Z. Bai, A. Saha, W. Yuan, J. S. Walling, University of Utah

In this paper, we introduce the multiphase switched-capacitor power amplifier (MP-SCPA). The MP-SCPA is a digital power amplifier (DPA) that achieves a linear output response using a vector summation of two amplitude weighted constant phase signals. In this way, it avoids using a wideband phase modulator that is required in other DPAs. The MP-SCPA is subject to non-linearity induced by bondwires and other packaging associated inductance that causes variation in the voltage supply available on-chip. To correct for this packaging based non-linearity, we propose a polar digital pre-distortion that is more robust and requires less chip area than traditional lookup table based methods. A prototype MP-SCPA is measured with the polar DPD and found to have similar performance when compared with a dense lookup table based DPD. The MP-SCPA is measured with a 5 MHz, 64 QAM LTE signal and achieves a measured ACLR < -30 dBc, an EVM=3.4%-rms and an average system efficiency of 15.8%.

Session 7 - Data Converter Techniques
Monday, May 1, 1:30 - 5:30, Lady Bird 2 Room
Session Chair: Ayman Shabra, MediaTek
Session Co-Chair: Dong-Young Chang, Maxim

7-1 **A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration**, Yeonam Yoon, Nan Sun, University of Texas at Austin

This paper presents a 6-b high-speed SAR ADC with sparkle code correction. By quantizing the comparator decision time, sparkle codes are corrected. Furthermore, CDT quantization enables 1-bit increase in ADC resolution. A novel dither-based background calibration technique is devised to accurately control the CDT detection window and ensure PVT robustness.

7-2 **A Pipelined SAR ADC Reusing the Comparator as Residue Amplifier**, M. Gandara, W. Guo, X. Tang, L. Chen, Y. Yoon, N. Sun, University of Texas-Austin

This paper presents a 12-bit pipelined SAR ADC that reuses the comparator from the first-stage SAR to perform residue amplification. The proposed amplifier utilizes positive feedback to achieve a large gain at high speed. To the authors' knowledge, this work achieves the highest interstage gain of any reported dynamic amplifier.

7-3 **A 74.33 dB SNDR 20 MSPS 2.74 mW Pipelined ADC using a Dynamic Deadzone Ring Amplifier**, S. Leuenberger, J. Muhlestein, H. Sun, P. Venkatachala, U. Moon, Oregon State University

This work is a ring amplifier built with current-starved inverters in the intermediate stage. This structure combined with a dynamic deadzone combines the properties of both coarse estimation and fine settling. The ADC consumes 2.74 mW and achieves a peak SNDR of 74.33 dB which provides a FoM of 32.2 fJ/c-step.

7-4 **A 12-/14-bit, 4/2MSPS, 0.085mm2 SAR ADC in 65nm Using Novel Residue Boosting**, Joonsung Park, Krishnaswamy Nagaraj, Mikel Ash*, Ajay Kumar**, Texas Instruments, *Cirrus Logic, **Microchip

In this paper, a re-configurable 12/13/14-bit SAR ADC based on a 12-bit ADC core is presented. A novel residue-boosting algorithm is developed to increase the bit resolution of a SAR ADC up to 2 bits without significant additional area and power. In the 12-bit mode, the 65nm prototype shows both DNL and INL of about +/- 0.5 LSB at 4MSPS, and in 14-bit mode, DNL and INL are about +/- 1 LSB and +/- 2 LSB at 2MSPS. ENOB is 11.5 bit and 13 bit for 12-bit and 14-bit mode each. The area of the ADC is 0.085mm2.

7-5 **A Background Calibrated 28GS/s 8b Interleaved SAR ADC in 28nm CMOS**, Michael Q. Le, James Gorecki, Jamal Riani, Jorge Pernillo, Amber Tan, A. Buchwald, Karthik Gopalakrishnan, Belal Helal, Pulkit Khandelwal, ChangFeng Loi, Irene Quek, Pui Wong

Abstract—A 28-GS/s time-interleaved ADC suitable for PAM4 optical and backplane applications is presented. The architecture uses a two-rank 2x(4:4) sampling network to interleave 32 8b SAR ADCs employing redundancy to relax DAC settling requirements. A DSP core estimates and corrects the gain, offset and timing error between channels. An ENOB of 5.8b and 5.4b is achieved with 1-GHz and 13.3GHz input signals. The ADC consumes 165-mW from a single 950-mV power supply and is fabricated in a 28nm CMOS process occupying 0.24mm2.

7-6 **A 10-b 2b/cycle 300MS/s SAR ADC with a Single Differential DAC in 40nm CMOS**, J. Song, X. Tang, N. Sun, University of Texas at Austin

This paper presents a 300MS/s single-channel 2b/cycle hybrid SAR with only 1 differential DAC. The proposed architecture exploits both differential and common mode voltages to generate 3 comparison levels needed for 2b/cycle without requiring extra DAC. It achieves peak 8.5b ENOB and consumes 2.1mW. FoM of 19.3fJ/conv-step is achieved.

7-7 **A 73dB SNDR 20MS/s 1.28mW SAR-TDC Using Hybrid Two-Step Quantization**, J. Muhlestein, S. Leuenberger, H. Sun, Y. Xu, U. Moon, Oregon State University

A Hybrid SAR-TDC technique offers scalability, simplicity and efficiency. Quantization is performed on both voltage and time domain signals. Measured prototype demonstrates an SNDR of 73 dB at 20 MSPS and 1.28 mW power for a Walden Figure of merit of 17.4 fJ/conversion-step.

Session 8 - Biomedical Circuits and Systems
Monday, May 1, 1:30 - 5:30, Lady Bird 3 Room
Session Chair: Pedram Mohseni, Case Western Reserve University
Session Co-Chair: Kaushik Sengupta, Princeton University

8-1 **Design of Miniaturized Wireless Power Receiver for mm-sized implants**, Chul Kim, Sohmyung Ha*, Jiwoong Park, Abraham Akinin, Rajkumar Kubendran, Hui Wang, Patrick P. Mercier, Gert Cauwenberghs, University of California, San Diego, *New York University Abu Dhabi

Current WPT technique relies on bulky power receiving (RX) coil and power storage decoupling capacitors, disturbing the realization of mm-sized implants. Ultimate miniaturization is possible by integrating such external bulky components into on-chip wireless power receivers. In this paper, two fully integrated wireless power receiver for mm-sized implants are introduced.

8-2 **A Power-Efficient Multi-Channel PPG ASIC with 112dB Receiver DR for Pulse Oximetry and NIRS**, P. Schönle, S. Fateh, T. Burger, Q. Huang, ETH Zurich

The chip supports probes with up to 32 LEDs and 4 photodiodes and features a receiver that covers a wide input current range. A higher power-efficiency than the state-of-the-art results in 68% less total power consumption (incl. LEDs) for equal performance or 7dB higher performance at equal power consumption.

8-3 **A Dynamically Reconfigurable ECG Analog Front-End with a 2.5× Data-Dependent Power Reduction**, Somok Mondal, Chung-Lun Hsu, Roozbeh Jafari*, Drew Hall, University of California, San Diego, *Texas A&M University

An analog front-end (AFE) with agile, on-the-fly noise-power reconfiguration for data-dependent power savings of 2.5× is presented. Implemented in 65nm CMOS the AFE offers programmable noise from 1.90-2.91 µVrms while consuming 307-769 nW power and is assisted by an LMS-based adaptive linear predictive filter to exploit low-activity and quasi-periodicity of bio-signals.

8-4 **CMOS Sensor for Dual Fluorescence Intensity and Lifetime Sensing Using Multicycle Charge Modulation**, Guoqing Fu, Sameer Sonkusale, Tufts University

A novel CMOS sensor chip is proposed to realize both fast and accurate intensity and lifetime sensing for fluorescence. CTIA-based multi-cycle charge modulation achieves 4.38nW/cm2 resolution for intensity measurement and 45ns resolution for lifetime measurement. Dissolved oxygen is measured with 7.5%/ppm and 6%/ppm sensitivity in both intensity and lifetime domain.

8-5 **A 255nW Ultra-High Input Impedance Analog Front-End for Non-contact ECG Monitoring**, Jinseok Lee, Hyojun Kim, SeongHwan Cho, KAIST

In this paper, we propose a high input impedance analog front-end for low-power biopotential acquisition. All of parasitic capacitance including off-chip, PAD, ESD, and transistor gate at the input were cancelled using positive feedback. A prototype IC fabricated in 0.18µm CMOS consumes 255nW and has input capacitance of 60fF.

8-6 **A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for Forward-Looking Intravascular Ultrasound**, Mingliang Tan*, Chao Chen*, Zhao Chen*, Jovana Janjic**, Verya Daeichin**, Zu-yao Chang*, Emile Noothout***, Gijs van Soest**, Martin Verweij***, Nico de Jong**,*** and Michiel Pertijs*
*Electronic Instrumentation Laboratory, Delft University of Technolo

This paper presents a front-end ASIC for forward-looking intravascular ultrasound imaging. It is intended to be mounted at the tip of a catheter and interfaces 80 piezo-electric transducer elements with an imaging system using only 4 cables, thus significantly reducing the system complexity compared to the prior art.

8-7 **Interference-immune Diagnostic Quality ECG Recording for Patient Monitoring Applications**, A. Kalb, Y. Sharma, Analog Devices Inc.

This paper describes an ECG conversion channel providing diagnostic quality readouts while under severe interference. The input dynamic range is greater than ±1 V with an overload recovery time of approximately 12 ms. Input bias currents are maintained below 150 pA. The noise per channel is approximately 1.2 µVrms.

8-8 **A CMOS 22k-Pixel Single-Cell Resolution Multi-Modality Real-Time Cellular Sensing Array**, J. Park, M. Aziz, S. Gonzalez*, D. Jung, T. Chi, S. Li, H. Cho*, H. Wang, Georgia Tech, *Emory University

This paper presents a 22k-pixel multimodality sensing array with a DCCA for cell characterization and drug screening. DCCA achieves the measured input-referred noise of 2.46μVrms and cell-based measurements successfully capture the beating rate of cardiomyocytes using both optical detection and potential recording. Additionally, drug effects of isoproterenol are successfully characterized.

Session 9 - Panel - Hardware and Software Security: Gaps and Synergies
Monday, May 1, 1:30 - 5:30, Lady Bird Studio Room

Session 10 - Forum - MM-wave and Wide Band Circuits for 5G Communications and Automotive Radar
Monday, May 1, 3:30 - 5:30, Lady Bird 1 Room

Session 11 - Wireline Building Blocks
Tuesday, May 2, 9:00 - 12:00, Lady Bird 1 Room
Session Chair: Eric Naviasky, Cadence
Session Co-Chair: Mohammad Hekmat, Samsung

11-1 **A 10 GHz 56 fsrms-Integrated-Jitter and -247 dB FOM Ring-VCO Based Injection-Locked Clock Multiplier with a Continuous Frequency-Tracking Loop in 65 nm CMOS**, Xuqiang Zheng, Fangxu Lv, Feng Zhao*, Shigang Yue*, Chun Zhang, Ziqiang Wang, Fule Li, Hanjun Jiang, Zhihua Wang, Tsinghua University, *University of Lincoln

This paper develops a 10GHz Ring-VCO based injection-locked clock multiplier (RILCM) using a new timing-adjusted PD based hybrid frequency tracking loop in 65nm CMOS. The measured results show that it achieves 56.1fs rms-jitter and -57.13dBc spur level. The calculated figure-of-merit (FOM) is -247.3dB.

11-2 **Jitter Injection for On-Chip Jitter Measurement in PI-Based CDRs**, J. Liang, A. Sheikholeslami, University of Toronto
H. Tamura, H. Yamaguchi, Fujitsu Laboratories Limited

The RMS relative jitter between the clock and data of a 28Gb/s half-rate PI-based digital CDR fabricated in 28nm CMOS, is measured with sub-picosecond accuracy by injecting square wave jitter using the CDR's PI code and measuring its effect on the autocorrelation function of the bang-bang PD output.

11-3 **A 27.1 mW, 7.5-to-11.1 Gb/s Single-Loop Referenceless CDR With Direct Up/dn Control**, K. Park, W. Bae, D.-K. Jeong, Seoul National University

A 7.5-to-11.1 Gb/s half-rate referenceless CDR with a compact frequency acquisition scheme is proposed. Using the bang-bang phase-frequency detector with a direct up/dn control, the referenceless CDR is realized by a single-loop architecture. The proposed CDR achieves a wide capture range, low power, and small area.

11-4 **A 40-Gbps 0.5-pJ/bit VCSEL Driver in 28nm CMOS with Complex Zero Equalizer**, A. Sharif-Bakhtiar, M. G. Lee*,A. Chan Carusone, University of Toronto, *Fujitsu Labs of America

The paper explains a 40Gbps VCSEL driver in 28nm CMOS technology achieving 1.3dBm OMA at record low 0.5pJ/b power efficiency. The transmitter utilizes a new type of low-power equalizer with a pair of tunable complex zeros in its transfer function to compensate for VCSEL electro-optical ringing enabling 40Gbps operation.

11-5 **Low-Power CMOS Receivers For Short Reach Optical communication**, A. Sharif-Bakhtiar, M. G. Lee*,A. Chan Carusone, University of Toronto, *Fujitsu Labs of America

The paper explains the motivation behind low-bandwidth frontend optical receivers in CMOS. Reported receivers with low bandwidth frontends utilizing DFE, CDS, and integrate-and-dump (ID) are analyzed. Finally design of an ID receiver fabricated in 28nm CMOS with -8.5dBm sensitivity and 0.7pJ/b power efficiency at 20Gbps is explained.

Session 12 - Analog Techniques I
Tuesday, May 2, 9:00 - 12:00, Lady Bird 2 Room
Session Chair: Nagendra Krishnapura, IIT Madras
Session Co-Chair: Ken Suyama, Epoch Microelectronics

12-1 **A 0.5V Supply, 49nW Band-Gap Reference and Crystal Oscillator in 40nm CMOS**, Abhirup Lahiri, Pradeep Badrathwal, Nitin Jain, Kallol Chatterjee, STMicroelectronics

Operating from 0.5V supply, a band-gap reference (BGR) and 32kHz crystal oscillator (XO) are co-designed in 40nm CMOS process with <49nW power consumption from -40°C to 120°C and temperature coefficients of 8ppm/°C and 0.25ppm/°C, respectively. The power consumptions of both XO and BGR at 120°C are 2x lower than previous works.

12-2 **A Start-up Boosting Circuit with 133x Speed Gain for 2-Transistor Voltage Reference**, Dongkwun Kim, Wanyeong Jung, Sechang Oh, Kyojin D. Choo, Dennis Sylvester, David Blaauw, University of Michgan

This work presents a start-up boosting circuit designed for fast stabilization of a 2-transistor voltage reference. A clock injection method is used to induce a large bias on the 2-transistor voltage reference resulting in a fast output voltage settling which is critical to reducing initialization time and energy consumption.

12-3 **A Precisely-Timed Energy Injection Technique Achieving 58/10/2µs Start-Up in 1.84/10/50MHz Crystal Oscillators**, H. Esmaeelzadeh, S. Pamarti, University of California, Los Angeles

A fast start-up crystal oscillator using a precisely-timed injection technique is proposed. The prototype 65nm CMOS IC includes 3 crystal oscillators, targeting 1.84/10/50MHz with measured start-up times of 58/10/2µs while consuming 6.7/45.5/195µW respectively. This corresponds to 15x faster start-up over prior art. For each oscillator, two crystals with different package sizes and Q-factors were tested to verify the technique's robustness over crystal's parameters and frequency variations.

12-4 **A 0.7V Time-based Inductor for Fully Integrated Low Bandwidth Filter Applications**, B. Salz, M. Talegaonkar*, G. Shu**, A. Elmallah, R. Nandwana, B. Sahoo, P. K. Hanmolu, University of Illinois at Urbana-Champaign, *InPhi, **Oracle

A fully digital inductor is demonstrated in 65nm CMOS with wide tuning range and small area. The proposed technique uses novel time-domain signal processing techniques in order to generate an inductance. By realizing the gyrator like so, we are able to achieve small area and take advantage of technology scaling.

12-5 **A 0.65mW 20MHz 5th-Order Low-Pass Filter with +28.8dBm IIP3 Using Source Follower Coupling**, Y. Xu, J. Muhlestein, U. Moon, Oregon State University

A highly linear continuous-time low-pass filter (LPF) topology using source follower coupling is presented with excellent power efficiency. It synthesizes a 3rd-order low-pass transfer function in a single stage using coupled source followers and three capacitors, and can be configured to 2nd-order by disconnecting a capacitor. A 5th-order Butterworth prototype is designed with a cascade of two stages in 0.18µm CMOS, and occupies a

core area of 0.12mm2. Operating with a 1.3V supply, the filter consumes 0.5mA current, and achieves a bandwidth of 20MHz with 82dB stop-band rejection. The measured in-band IIP3 is +28.8dBm. The dynamic range is 74dB, with 15.3nV/√Hz averaged in-band input-referred noise.

Session 13 - Security Circuits and Systems
Tuesday, May 2, 9:00 - 12:00, Lady Bird 3 Room
Session Chair: Swaroop Ghosh, Pennsylvania State University
Session Co-Chair: Xin Li, Carnegie Mellon

13-1 **Energy Efficient and Ultra Low Voltage Security Circuits for Nanoscale CMOS Technologies**, Sanu Mathew, Sudhir Satpathy, Vikram Suresh, Ram K. Krishnamurthy, Circuit Research Lab, Intel Corporation

Low-area energy-efficient security primitives are key building blocks for enabling end-to-end content protection, user authentication, and consumer confidentiality in the IoT world that is estimated to surpass 50billion smart and connected devices by 2020. This paper describes design approaches that blend energy-efficient circuit techniques with optimal accelerator micro-architecture datapath, and hardware friendly arithmetic to achieve ultra-low energy consumption in security platforms for seamless adoption in area/battery constrained and self-powered systems. Industry leading energy-efficiency is demonstrated with three designs, fabricated and measured in advanced process technologies : 1) A 2040-gate arithmetically optimized composite-field Sbox based AES accelerator achieves 289Gbps/W peak energy-efficiency while offering 432Mbps throughput in 22nm tri-gate CMOS, 2) Hybrid Physically Unclonable Function (PUF) circuit leverages burn-in induced aging to reduce bit-error, followed by temporal-majority-voting, dark-bit masking, and error-correction conditioning techniques to generate a 100% stable full-entropy key with 190fJ/bit energy consumption in 22nm tri-gate CMOS. 3) A light-weight all digital TRNG uses in-line correlation suppressor and entropy-extractor circuits to achieve >0.99 min-entropy with 3pJ/bit measured energy-efficiency while operating down to 300mV in 14nm tri-gate CMOS.

13-2 **A DRAM based Physical Unclonable Function Capable of Generating >10^32 Challenge Response Pairs per 1Kbit Array for Secure Chip Authentication**, Qianying Tang, Chen Zhou, *Woong Choi, *Gyuseong Kang, *Jongsun Park, Keshab Parhi, and Chris. H. Kim, University of Minnesota,*Korea University

A Physically Unclonable Function (PUF) based on a 65nm logic-compatible DRAM achieves a higher level of security compared to previous memory based PUFs by supporting >10^32 possible challenge response pairs per 1Kbit array. Hardware data shows an intra-chip Hamming Distance (HD) of 0.0039 by utilizing a zero-overhead repetitive write-back technique along with bit-masking. The proposed eDRAM based PUF has a 0.68μm^2 bit cell area and consumes 0.89pJ/bit.

13-3 **Trustworthy System-on-Chip Design for Internet of Things**, Sandip Ray, NXP Semiconductors

The Internet of Things (IoT) regime arguably began about a decade back, when the number of connected computing devices exceeded the human population. Today our environment includes billions of connected devices, coordinating and communicating to implement applications of the scale of intelligent homes, self-driving automobiles, and smart cities. The trend is towards even more proliferation of these devices with estimates of trillions within the next 15 years, representing the fastest growth for any sector at any time in the human history. Security and trustworthiness are critical requirements for computing systems in IoT applications. In particular, these systems track, collect, and analyze some of our most private, personal information including health, sleep patterns,

contact information, browsing patterns, etc. In addition, the system may contain other sensitive assets built-in by the manufacturer, e.g., cryptographic and DRM keys, fuses, etc. It is crucial to ensure that all such sensitive information is protected from malicious, unauthorized access. Consequently, a significant component of development of a modern System-on-Chip (SoC) design is expended on architecting, designing, and validating security mechanisms. In this talk, we will look at security assurance challenges for modern SoC designs targeted for Internet-of-Things applications. Security assurance mechanisms in current industrial practice is a highly complex activity, spanning the entire system life-cycle, and involving trade-offs and collaboration among a large number of stake-holders. We will discuss the gaps between the current state of the practice and the assurance requirements, and some of the research initiatives undertaken to bridge these gaps. Research in the area marries several research topics in computer science and engineering, including architecture, power/performance management, hardware/software co-design, and verification, and the talk will give a flavor of the nature of the cross-cutting research necessary to develop trustworthy computing devices in the IoT era.

13-4 **An Area-Efficient Microcontroller with an Instruction-Cache Transformable to an Ambient Temperature Sensor and a Physically Unclonable Function**, Teng Yang, Jiangyi Li, Minhao Yang, Peter R. Kinget, Mingoo Seok, Columbia University

This paper presents an very area-efficient SoC design with ambient temperature sensing and PUF operations based on a unique transformation of microcontroller's I$ to temperature sensor and PUF. It has comparable performances to the state-of-the-art but consumes 9.8X smaller sensor frontend area.

Session 14 - Forum - Self-Sustaining IoTs - Fact or Fiction
Tuesday, May 2, 9:00 - 12:00, Lady Bird Studio Room

Session 15 - Energy Efficient Wireless for 5G and IoT
Tuesday, May 2, 2:00 - 5:30, Lady Bird 1 Room
Session Chair: Woogeun Rhee, Tsinghua University
Session Co-Chair: Swaminathan Sankaran, Texas Instruments

15-1 **Energy Efficiency Maxima for Wireless Communications: 5G, IoT, and Massive MIMO**, Earl McCune, Eridan Communications

Maximum energy efficiency of any wireless communication link requires a global optimization across the entire block diagram, the signal modulation, and the link operating protocol. Important aspects of signal modulation are presented, followed by protocol aspects needed for link efficiency. Operating temperature consequences of LTE for massive-MIMO arrays are explored.

15-2 **An Ultra-Low-Power Wake-Up Receiver with Voltage-Multiplying Self-Mixer and Interferer-Enhanced Sensitivity**, Vivek Mangal, Peter R. Kinget, Columbia University

A 0.5V self-mixer-first 550MHz 220nW wake-up receiver in 0.13um CMOS has a -56.4dBm sensitivity at 36.36kbps and an energy consumption of 6.1pJ/bit. A 10-stage voltage-multiplying self-mixer using MOS transistors in weak inversion consumes 2.7nW and offers multi-stage conversion gain at baseband. In the presence of a -43.5dBm PM interferer, the alternate 1.1uW high-frequency baseband path in the receiver offers an enhanced sensitivity of -63.6dBm.

15-3 **A 6.1mW 5Mb/s 2.4GHz Transceiver with F-OOK Modulation for High Bandwidth and Energy Efficiencies**, Y. Zhang, R. Zhou, W. Rhee, Z. Wang, Tsinghua University

This paper presents an energy/bandwidth efficient frequency-domain OOK (F-OOK) transceiver for short-range communications. The transmitter performs the F-OOK modulation using a PLL based high-point modulator and a constant-envelope PA for low power consumption. The receiver consists of a sliding-IF RF front end and an 8-bit dual-channel ADC. A digital signal processing is done by an off-chip FPGA to provide F-OOK demodulation with an interference robust algorithm based on sliding-window FFT and magnitude comparison methods. A 2.4GHz 5Mb/s frequency-domain OOK (F-OOK) transceiver is implemented in 65nm CMOS. The sensitivity is -96dBm at 5Mb/s. The transceiver consumes 6.1mW from a 0.8V, achieving an energy efficiency of 1.22nJb/s with the bandwidth efficiency of 96%.

Session 16 - Switching Regulators
Tuesday, May 2, 2:00 - 5:30, Lady Bird 2 Room
Session Chair: Jeff Morroni, Texas Instruments
Session Co-Chair: Mike Mulligan, Silicon Laboratories

16-1 **A Digital Pulse Width Modulation Closed Loop Control LDMOS Gate Driver for LED Drivers Implemented in a 0.18µm HV CMOS Technology**, S. Strache, L. Rolff*, S. Dietrich*, M. Hanhart*, T. Zekorn*, R. Wunderlich*, S. Heinen*, Robert Bosch GmbH, *RWTH Aachen University

For multicolor LED driver applications several integrated HV transistors have to be driven. The presented digital PWM gate driver is based on GCM and employs a digital centric closed loop gate-source voltage control. It directly drives the transistors out of the HV supply without requiring external components.

16-2 **A 10MHz 2mA-800mA 0.5V-1.5V 90% Peak Efficiency Time-Based Buck Converter with Seamless Transition between PWM/PFM Modes**, S. J. Kim, W. Choi, R. Pilawa, P. K. Hanumolu, University of Illinois at Urbana-Champaign

We present a 10MHz buck converter with enhanced light load efficiency achieved by combining time-based PWM control with PFM. The proposed seamless transition techniques provide freedom of exchanging the control mode between PFM and PWM which greatly enhance system power management. Fabricated in a 65nm CMOS, the prototype achieves 90% peak efficiency and > 80% efficiency over load current range of 2mA to 800mA. VO changes by less than 40mV during PWM to PFM transitions.

16-3 **An isolated DC-DC converter with fully integrated magnetic core transformer**, Zhao Tianting, Zhuo Yue, Chen Baoxing, Analog Devices

This work presents an isolated DC-DC converter with fully integrated magnetic core transformer. The converter achieves best-in-class efficiency (46%) and EMI performance (pass CISPR22 Class B limit with 10dB margin).

16-4 **A 92.1% Efficient DC-DC Converter for Ultra-Low Power Microcontrollers with Fast Wake-up**, F. Santoro, R. Kuhn*, N. Gibson*, N. Rasera*, T. Tost*, D. Schmitt-Landsiedel, R. Brederlow*, TUM, Munich, Germany, *Texas Instruments, Freising, Germany

We present a DC-DC converter (1.8-3.3V input / 1.2V output) for integration in an ultra-low power system on chip. The converter is designed to minimize the wake-up energy of the system by reducing the output cap to only 56nF - still guaranteeing an output ripple smaller than 30mV at 2.56mA load.

16-5 **Buck Converter with Higher Than 87% Efficiency over 500nA to 20mA Load Current Range for IoT Sensor Nodes by Clocked Hysteresis Control**, C.-S. Wu, M. Takamiya, T. Sakurai, The University of Tokyo

A buck converter with newly proposed Clocked Hysteresis Control has been developed that achieves conversion efficiency of 90.4% at 1μA load current and almost flat efficiency in whole load current range. Continuously-on comparators in the conventional hysteresis control is removed to improve the conversion efficiency under light load current conditions while maintaining a fast transient response.

16-6 **A 220-mV Input, 8.6 Step-Up Voltage Conversion Ratio, 10.45-□W Output Power, Fully Integrated Switched-Capacitor Converter for Energy Harvesting**, Luca Intaschi, Francesco Dalena*, Paolo Bruschi, Giuseppe Iannaccone, University of Pisa, Dialog Semiconductor

We present a 10.45 □W fully integrated step-up switched-capacitor DC-DC converter for energy harvesting, with 8.6 voltage-conversion ratio and 37.4% power-conversion efficiency from a 220 mV voltage source. The circuit, implemented in 55nm CMOS, can supply power to a Bluetooth beacon with a thermoelectric generator exploiting a 3.5°C temperature difference.

16-7 **A 1.2A Auto-Configurable Dual-Output Switched-Capacitor DC-DC Regulator with Continuous Gate-Drive Modulation Achieving ≤0.01mV/mA Cross Regulation**, Z. Hua and H. Lee, University of Texas at Dallas

An auto-configurable 2-output SC DC-DC regulator in 0.13μm CMOS is reported. The continuous gate-drive modulation allows the converter being the first capable of handling 100s-of-mA load/output with minimized output cross regulation (OCR) and the use of small required load capacitance. The proposed regulator supports 600mA/output load with only a 2.2μF capacitor, offers 87.6% peak power efficiency, and achieves >4x and 3.4x reductions in the OCR and total passive volume compared to prior SIMO converters.

16-8 **Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Ranges**, Saurabh Chaubey
Ramesh Harjani

This paper presents a fully integrated, software defined capacitive DC-DC converter. The converter implements K-F-C tuning (K = conversion ratio, F = frequency and C = capacitance) in real time so as to accommodate any output load. It has a 4X tunable output voltage, supports a 3269X output load current range while achieving a peak efficiency of 82.1%. This design introduces an accumulation floating junction MOS capacitor that is used for the 18.3 fF/ m2 bucket-capacitors with less than 2 A/mm2 leakage. This leakage is 40X lower than standard MOS capacitors. The converter transforms a 1.0V input to a 0.25-0.95V output for a 0.13mA-425mA load range while maintaining better than 70% efficiency. The power density for better than at 70% efficiency is 1.05W/mm2 (@ Vout=430mV). Load regulation is implemented using capacitive and frequency tuning in digital and analog domains respectively. The design was fabricated in TSMC GP 65nm.

Session 17 - Non-Traditional Computing Hardware
Tuesday, May 2, 2:00 - 5:30, Lady Bird 3 Room
Session Chair: Axel Thomsen, Cirrus Logic
Session Co-Chair: Dinesh Somasekhar, Intel

17-1 **Hardware for Machine Learning: Challenges and Opportunities**, V. Sze, Y.-H. Chen, J. Emer, A. Suleiman, Z. Zhang, Massachusetts Institute of Technology

17-2 **A Scalable Time-based Integrate-and-Fire Neuromorphic Core with Brain-Inspired Leak and Local Lateral Inhibition Capabilities**, Muqing Liu, Luke R. Everson, and Chris H. Kim, University of Minnesota

A fully scalable light-weight integrate-and-fire neuromorphic core with brain-inspired leak and local lateral inhibition features is implemented in 65nm. The core computes the neural net algorithm entirely in the time domain using standard digital circuits. A parallel two-layer architecture realized using the proposed core achieves a 91% digit recognition accuracy.

17-3 **Temperature-Insensitive Analog Vector-by-Matrix Multiplier Based on 55 nm NOR Flash Memory Cells**, X. Guo, F. Merrikh Bayat, M. Prezioso, Y. Chen*, B. Nguyen*, N. Do*, D. B. Strukov, UC Santa Barbara, *Silicon Storage Technology Inc.

We have fabricated , 85 °C.

17-4 **Analog In-Memory Subthreshold Deep Neural Network Accelerator**, L. Fick, D. Blaauw, D. Sylvester, University of Michigan, S. Skrzyniarz, M. Parikh, D. Fick, Isocline Engineering

Low duty-cycle mobile systems could benefit from ultra-low power DNN accelerators. Analog in-memory computational units store synaptic weights in on-chip non-volatile arrays to perform subthreshold current calculations. In-memory computation entirely eliminates off-chip weight accesses and amortizes read power through current re-use. The proposed system consumes 900nW in a 130nm process.

17-5 **A 4-mm^2 180-nm-CMOS 15-Giga-Cell-Updates-per-Second DNA Sequence Alignment Engine Based on Asynchronous Race Conditions**, A. Madhavan, T. Sherwood, D. B. Strukov, University of California, Santa Barbara

2X2mm chip of a Race Logic based system, which uses race conditions for accelerating DNA sequence alignment. In Race Logic, information is encoded in propagation delay and the computation is performed by observing outcome of races in a configurable circuit. Performance and power results reported show favourable comparison against state-of-the-art.

17-6 **Using Quantum Emulation for Advanced Computation**, Brian R. La Cour, Granville E. Ott, S. Andrew Lanham, Applied Research Laboratories, The University of Texas at Austin

A novel concept for advanced computation is considered using an analog electronic emulation of a gate-based quantum computer. We discuss a general classes of problems for which such a device is well suited, examine the expected computational speedup versus bandwidth, and describe the measured performance of a small-scale hardware prototype.

Session 18 - Panel - Your Favorite Analog/Mixed-signal/RF Circuits
Tuesday, May 2, 2:00 - 5:30, Lady Bird Studio Room

Session 19 - High-Performance and Low-Power Frequency Generation
Tuesday, May 2, 2:00 - 5:30, Lady Bird 1 Room
Session Chair: Yanjie Wang, Intel
Session Co-Chair: Hua Wang, Georgia Tech

19-1 **Multi-Phase Sub-Sampling Fractional-N PLL with Soft Loop Switching for Fast Robust Locking**, Dongyi Liao, Fa Foster Dai, Bram Nauta*, and Eric Klumperink*, Dept.

of Electrical and Computer Eng., Auburn University, USA *University of Twente, Enschede, Netherlands

This paper presents a low phase noise sub-sampling PLL (SSPLL) with multi-phase outputs. Automatic soft switching between the sub-sampling phase loop and frequency loop is proposed to improve robustness. A quadrature LC oscillator with capacitive phase interpolation network is employed to achieve fractional-N frequency synthesis.

19-2 **A 0.8-1.3 GHz Multi-phase Injection-locked PLL Using Capacitive Coupled Multi-ring Oscillator with Reference Spur Suppression**, Ruixin Wang, Fa Foster Dai, Auburn University

This paper presents an inductor-less injection-locked PLL (IL-PLL) using capacitive coupled multi-ring oscillator (MRO). With a 50 MHz reference, the MRO IL-PLL generates 24 multi-phase outputs covering 800-1.3 GHz with reference spur of -63 dBc,in-band phase noise of -121 dBc/Hz @ 1MHz offset and 513 fs jitter.

19-3 **A 330μW 1.25ps 400fs-INL Vernier Time-to-Digital Converter with 2D Reconfigurable Spiral Arbiter Array and 2nd-Order ΔΣ Linearization**, H. Wang*, F. F. Dai*, H. Wang**, *Auburn University, **Georgia Institute of Technology College of Engineering

Paper presents an 8-bit 1.25ps Vernier TDC with 2D reconfigurable spiral arbiter array. The 2D spiral arbiter array improves both linearity and detection range. The quantization errors are minimized using a reconfigurable arbiter array with 2nd order SDM. The prototype consumes 0.3mW under a 1V supply achieving 0.4ps INL.

19-4 **A 350uW 2GHz FBAR transformer coupled Colpitts oscillator with close-in phase noise reduction**, Jabeom Koo, Keping Wang, Richard Ruby*, Brian Otis, University of Washington, *Avago technologies Inc.

The proposed oscillator reduces the close-in phase noise as well as power consumption compared to conventional Colpitts by utilizing transformer. Measurement results show 12dB reduction at 100Hz offset frequency with 350uW power consumption, which is almost a half power of conventional oscillator using same 2GHz FBAR device.

Session 20 - High-Performance Low-Power Wireless Receivers
Wednesday, May 3, 9:00 - 12:00, Lady Bird 1 Room
Session Chair: Julian Tham, Broadcom
Session Co-Chair: Hossein Lavasani, Georgia Tech

20-1 **N-path filters and Mixer-First Receivers: A Review**, E.A.M. Klumperink, H.J. Westerveld, Bram Nauta, University of Twente

To realize a Software Defined Radio covering the mainstream 0.5-6 GHz wireless communication bands, new SAW-less radio receiver architectures are being explored which realize selectivity in a more flexible and programmable fashion. N-path filters and mixer-first receivers can offer high-linearity high-Q RF-filtering around a center frequency defined by a digital clock, which offers the desired flexible programmability. This paper reviews recent research on N-path filters and mixer-first receivers, identifies advances in performance analysis, circuit performance and applications.

20-2 **A Digital Sine-Weighted Switched-Gm mixer for Single-Clock Power-Scalable Parallel Receivers**, Reda Kasri* ** *** Eric Klumperink** , Philippe Cathelin*, Eric Tournier***,Bram Nauta**,*STMicroelectronics, Crolles, France, **University of Twente, Enschede, Netherlands,***LAAS-CNRS, UPS Université de Toulouse, Toulouse, France.

20-3 **A Scalable Architecture for Fully Integrated Multi-TV Tuners**, M. H. Koroglu, A. L. Coban, V. M. Pereira, F. Barale, S. X. Wu , W. Yu, R. Sun, and K. Pentakota Silicon Labs Inc.

Silicon TV tuners surpassed CAN-tuners, providing manufacturers with lower-cost, smaller and reliable solutions. Multi-tuners are needed in TVs and Set-Top-Boxes. This paper presents the major blocks for a monolithic dual-tuner with active splitter, tracking filters, buffers, low-power VCO based ADC and local oscillator featuring a 17GHz VCO with fractional dividers.

20-4 **A LTE RX Front-end with Digitally Programmable Multi-Band Blocker Cancellation in 28nm CMOS**, Q. Wang, H. Shibata*, A. Chan Carusone, A. Liscidini, University of Toronto, *Analog Devices

This paper presents a LTE receiver front-end with a feedback digital filter in the baseband to perform multiband blocker cancellation. The programmable filter provides 34.9dB attenuation of TX leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5MHz–107.5MHz. The receiver front-end operates at 1.8GHz with a noise figure of 3.9dB, IIP3 of -5dBm, and consumes only 20.4–37.5mW, the lowest among state-of-the-art designs.

20-5 **A 980µW 5.2dB-NF Current-Reused Fully Integrated Direct-Conversion Bluetooth-Low-Energy Receiver in 40nm CMOS**, A.Masnadi,H.Lavasani, M.Sharifzadeh, Y.Rajavi, M.Taghivand, S.Mirabbasi* , Qualcomm Inc , *University of British Columbia

Bluetooth Low Energy (BLE) is one of the most popular standards for ultra-low-power radios. Most BLE radios are based on power-hungry low-IF architectures. In this work, current-reuse and subthreshold techniques are employed to deliver a 980µW direct-conversion BLE receiver in 40nm CMOS with multiple µW-level feedbacks that make the design robust over PVT.

Session 21 - Analog Techniques II
Wednesday, May 3, 9:00 - 12:00, Lady Bird 2 Room
Session Chair: Farhan Adil, Massachusetts Institute of Technology
Session Co-Chair: Jiangfeng Wu, Tongji University

21-1 **A ±5V, ±10V, ±15V, 4-Channel Class-G Biphasic Constant-Current Stimulator**, E. Lee, Alfred Mann Foundation

A 4-channel class-G biphasic constant-current (CC) stimulator using ±5V, ±10V and ±15V supplies was proposed to improve average power efficiency (PE). Based on monitoring the output voltage (VSTO), output current would be drawn from different supplies. Bias currents for producing output were reused to monitor VSTO and to switch softly the current drawn from different supplies. Based on a 0.18µm process, the stimulator achieved an improvement of 35% on PE when compared to a conventional CC stimulator.

21-2 **From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing**, Siddharth Joshi, Chul Kim, Sohmyung Ha*, Gert Cauwenberghs, University of California San Diego, * New York University Abu Dhabi

Machine learning and related statistical signal processing algorithms are expected to transform sensor networks and greatly facilitate the Internet of Things. As such, incorporating these algorithms leads to oft-ignored architectures and presents a new set of design trade-offs. This paper considers the implementation of mixed-signal matrix-

vector multiplication as a central computational primitive enabling machine learning and statistical signal processing. We describe algorithms that can be implemented on such primitives in the presence of analog variation. We also briefly introduce emerging devices and technologies, providing examples of their use.

21-3 **Design of Tunable Digital Delay Cells**, Yu Chen, Rajit Manohar*, Yannis Tsividis, Columbia University, *Cornell University

This work discusses design considerations for tunable delay cells with good matching, low jitter, and robust communication interface. Effects resulting in signal-dependent delay are discussed and eliminated. A 1.2V 65nm prototype achieves a tunability range of 5n-10μs, with a matching standard deviation of 2.3% and jitter standard deviation of 0.065%.

21-4 **RC-Triggered ESD Clamp with Low Turn-on Voltage**, M. Stockinger, R. Mertens, NXP Semiconductors

We present circuit techniques for improving system-level ESD performance of RC-triggered boosted rail clamps. We lower the trigger voltage by switching a capacitor onto the RC detector stage. VDD stress is further reduced by adding a dedicated VDD detector stage. Test and simulation data of a CMOS microcontroller are included.

21-5 **A CMOS Pixel Design with Binary Space-time Exposure Encoding for Computational Imaging**, Y. Luo, S. Mirabbasi, University of British Columbia

A CMOS pixel design targeting to spatial-temporal exposure encoding based computational imaging is presented. By integration of selective charge storage units and exposure code memories, the prototyped pixel design performs both temporal and spatial-temporal encoded exposure.

22-1 **An 84 dB Dynamic Range 62.5-625 kHz Bandwidth Clock-Scalable Noise-Shaping SAR ADC with Open-Loop Integrator using Dynamic Amplifier**, M. Miyahara, A. Matsuzawa, Tokyo Institute of Technology

This paper proposes a noise shaping SAR ADC with open-loop integrator using dynamic amplifier. The proposed integrator requires low-gain open-loop amplifiers, therefore low power dynamic amplifier can be used. An SNDR of 83.5dB, a power consumption 273.4uW, and a FoM of 173dB with a bandwidth of 250kHz is achieved.

Session 22 - Oversampling Data Converter
Wednesday, May 3, 9:00 - 12:00, Lady Bird 3 Room
Session Chair: Nima Maghari, University of Florida
Session Co-Chair: Ivan O'Connell, University College Cork

22-2 **A 2.4mW, 111 dB SNR Continuous-time ΣΔ ADC With A Three-level DEM Technique**, Khiem Nguyen, Michael Determan, Analog Devices Inc.
Sejun Kim, Broadcom Corp.

A multi-bit continuous-time ΣΔ audio ADC employing 3-level unit-elements with 1st-order mismatch shaping which achieves 111dB A-weighted SNR, -98dB THD+N in the 22 kHz bandwidth, while consumes a total of 2.4mW from a 3.3V supply, and occupies ~0.5 mm2 in a 0.18um CMOS process

22-3 **A 50 MHz BW 73.5 dB SNDR Two-stage Continuous-time ΔΣ Modulator with VCO Quantizer Nonlinearity Cancellation**, S Dey, K Reddy*, K Mayaram, T Fiez**, Oregon State University, *Linear Technology Corporation, **University of Colorado Boulder

A 50MHz bandwidth two-stage continuous-time ΔΣ modulator with VCO-quantizer(VCOQ) is presented. The modulator suppresses the VCOQ Voltage-to-Frequency nonlinearity through dual path cancellation and achieves 73.5dB/88dB SNDR/SFDR. This architecture exhibit robustness against first stage quantization error leakage to the output. The SNDR variation remains within 1.5dB for ±10% gain mismatch between the two stages and temperature variation of 0C-80C.

22-4 **Adaptive Digital Noise-Cancellation Filtering using Cross-Correlators for Continuous-Time MASH ADC in 28nm CMOS**, Yunzhi Dong* ****, Jose B-Silva*, Qingdong Meng**, Jialin Zhao*, Wenhua Yang*, Trevor Caldwell***, Hajime Shibata***, Zhao Li***, Donald Paterson*, Jeffrey Gealow*, * Analog Devices, Wilmington, MA, ** Analog Devices, Cambridge, MA, *** Analog Devices, Toro

This paper presents an adaptive digital noise cancellation filter (DNCF) using cross-correlation (XCORR) developed for continuous-time (CT) multi-stage noise-shaping (MASH) ADCs. The XCORR engine continuously estimates the transfer functions of sub DS loops and updates the coefficients for the DNCF. An ADC prototype with this engine is built in 28nm CMOS and it achieves 72dB of dynamic range over 440MHz BW, with a total power of 1.25W from 1V and 1.8V supplies. Comparing to a power-up least-mean squares (LMS) engine, the XCORR-based adaptive DNCF achieves 2dB better noise cancellation across up to 10% supply variations.

22-5 **An 11.0 bit ENOB, 9.8 fJ/conv.-step Noise-Shaping SAR ADC Calibrated by Least Squares Estimation**, H. Garvik, C. Wulff, T. Ytterdal, Norwegian University of Science and Technology (NTNU)

A noise-shaping SAR ADC in 28 nm FDSOI, using an inverter-based loop filter is presented. A calibration technique that estimates CDAC calibration coefficients from a digitized test sequence is proposed. At Nyquist bandwidth 1.75 MHz, measured accuracy is 11.0 bit ENOB, and Walden FOM 9.8 fJ/conv.-step.

22-6 **A Two-Capacitor SAR-Assisted Multi-Step Incremental ADC with a Single Amplifier Achieving 96.6 dB SNDR over 1.2 kHz BW**, Y. Zhang, C.-H. Chen, T. He, Kazuki Sobue*, Koichi Hamashita*, and G. Temes, Oregon State University, *Asahi Kasei Microdevices

This paper presents a two-step incremental ADC (IADC) using SAR-assisted extended counting. In the first step, the IADC is configured as a first-order ΔΣ loop with an input feedforward architecture. In the second step, a two-capacitor SAR-assisted extended counting technique enhances the accuracy. A single active integrator is shared in both steps.

22-7 **A 1.2 V, 0.84 pJ/Conv.-Step Ultra-low Power Capacitance to Digital Converter for Microphone based Auscultation**, Neelakantan Narasimman*‡, Dipankar Nag‡, Kevin Chai Tshun Chuan‡, and Tony T. Kim* *VIRTUS, IC Design Centre of Excellence, School of EEE, Nanyang Technological University, Singapore, ‡ Institute of Microelectronics, A*STAR (Agency for Science, Technology

We propose a novel architecture and circuit implementation for Capacitance to Digital Converter. Capacitance information is digitized using a continuous time second order delta-sigma modulator with multi-bit quantization. Proposed architecture embeds a Capacitance to Voltage Converter in the delta-sigma loop, which improves dynamic range and energy efficiency of the CDC.

Session 23 - Panel - Bio-inspired Learning and Inference Systems: What Works Well and What Didn't

Wednesday, May 3, 9:00 - 12:00, Lady Bird Studio Room

Session 24 - Millimeter-Wave Communication Circuits
Wednesday, May 3, 1:30 - 5:30, Lady Bird 1 Room
Session Chair: John Long, University of Waterloo
Session Co-Chair: Fa Foster Dai, Auburn University

24-1 **Millimeter-wave Full-Duplex Wireless: Applications, Antenna Interfaces and Systems**, T. Dinc, H. Krishnaswamy, Columbia University

Millimeter-waves offer significantly wider channel bandwidths (BW) than RF and are drawing significant interest for short-range wireless personal area networks (WPANs), vehicular radar and next generation (5G) cellular communication. Full-duplex is another emergent technology which can theoretically double the spectral efficiency by transmitting and receiving simultaneously on the same frequency. This paper reviews recent developments at Columbia University on millimeter-wave full-duplex which merges these two emergent technologies. In this context, potential applications for millimeter-wave full-duplex links are described. A 60GHz full-duplex transceiver and 25GHz magnetic-free non-reciprocal passive circulator implemented in 45nm SOI CMOS process are discussed.

24-2 **A Bidirectional Lens-Free Digital-Bits-In/-Out 0.57mm2 Terahertz Nano-Radio in CMOS with 49.3mW Peak Power Consumption Supporting 50cm Internet-of-Things Communication**, Taiyun Chi, Hechen Wang*, Min-Yu Huang, Fa Foster Dai*, and Hua Wang, Georgia Tech, *Auburn University

A CMOS digital-bits-in/-out THz nano-radio with 0.57mm2 chip area is presented. The THz operation and bidirectional architecture lead to radio ultra-miniaturization. The TX harmonic oscillator is OOK- modulated, while an on-chip TDC measures RX oscillation start-up time for THz-to-bits receiving. It supports maximum 4.4Mb/s OOK over 50cm without Si lens.

24-3 **An Efficient 291 GHz Signal Source with 1.75 mW Peak Output Power in 65 nm CMOS**, A. Apriyana, G. Feng, S. Yang, Y. Liang, H. Yu, Nanyang Technological University
J. Wen, L. Sun, H. Yu, Hangzhou Dianzi University

A 291 GHz injection-locked signal source using two power-combined of 4-cell zero-phase coupled oscillator networks (CON) is demonstrated. The source exhibits 7.5% tuning range centered at 291 GHz or equivalently operating frequency range of 280 – 302 GHz and a peak output power of 1.75mW.

24-4 **An up to 36Gbps Analog Baseband Equalizer and Demodulator for mm-Wave Wireless Communication in 28nm CMOS**, O. E. Mattia*, D. Guermandi, G. Torfs, P. Wambacq*, Vrije Universiteit Brussel, Brussels, Belgium, *imec, Leuven, Belgium

In this paper we present, to the authors' best knowledge, the first complex DFE capable of equalizing 5 complex taps of inter-symbol interference on QPSK/16QAM data, at a maximum data-rate of 18/36Gbps, respectively, aggregating all 4 channels of the 60GHz IEEE802.11ad standard. This is realized with I and Q signal paths that can each handle 4PAM signals, leading to 16 possible constellation points to demodulate.

Session 25 - Linear Regulator Techniques
Wednesday, May 3, 1:30 - 5:30, Lady Bird 2 Room
Session Chair: Jeff Morroni, Texas Instruments
Session Co-Chair: Mike Mulligan, Silicon Laboratories

25-1 **Digitally-Assisted Leakage Current Supply Circuit for Reducing the Analog LDO Minimum Dropout Voltage**, Samantak Gangopadhyay, Saad Bin Nasir, *Hoan Nguyen, *Jihoon Jeong,*Francois Atallah, *Keith Bowman, Arijit Raychowdhury,School of ECE, Georgia Institute of Technology, GA, USA,*Qualcomm Technologies, Inc., Raleigh, NC, USA

A digitally-assisted leakage current supply (LCS) circuit reduces the maximum current demand for analog low-dropout (LDO) voltage regulators to lower the minimum dropout voltage (VDO,MIN), and consequently, enable a wider range of LDO operation for power savings in system-on-chip processor cores. From silicon measurements in a 130nm test chip, the LCS assisted hybrid LDO decreases VDO,MIN by 30-38%, resulting in core power reduction of 21-28% at equal clock frequencies within the wider LDO operating range.

25-2 **An External-Capacitor-less Low-Dropout Regulator with Less than –36dB PSRR at All Frequencies from 10kHz to 1GHz Using an Adaptive Supply-Ripple Cancellation Technique to the Body-Gate**, Younghyun Lim, Jeonghyun Lee, Suneui Park, Jaehyouk Choi, Ulsan National Institute of Science and Technology (UNIST)

This work presented an external-capacitor-less gate-dominant LDO that provides PSRR less than –36dB from 10kHz to 1GHz. Using an adaptive supply-ripple cancellation (ASRC) technique, the PSRR-hump of conventional gate-dominant LDOs was suppressed dramatically. Since the ASRC scaled ripples adaptively, the LDO maintained high PSRRs despite changes in load-current and dropout-voltage.

25-3 **Digitally Controlled Voltage Regulator Using Oscillator-based ADC with fast-transient-response and wide dropout range in 14nm CMOS**, Tarun Mahajan, Ramnarayanan Muthukaruppan, Dheeraj M. Shetty, Sumedha Mangal, Harish K. Krishnamurthy, Intel Corporation

This work targets 1-1.15V input voltage with output voltage range of 0.5-1.12V with minimum 30mV dropout, and load current range of >22x with 0.1-2.2A at 50mV dropout with <0.006mV/mA load regulation using 10-bit power-stage binary control and characterized using programmable synthetic resistive load with 18nF load capacitance on-die over load.

Session 26 - Forum - Emerging Techniques for Data Converters
Wednesday, May 3, 1:30 - 5:30, Lady Bird 3 Room

Session 27 - Technology Directions
Wednesday, May 3, 1:30 - 5:30, Lady Bird Studio Room
Session Chair: Christophe Antoine, Analog Devices
Session Co-Chair: Marco Tartagni, University of Bologna

27-1 **Flexible Selfbiased 66.7nJ/c.s. 6bit 26S/s Successive-Approximation C-2C ADC with Offset Cancellation using Unipolar Metal-Oxide TFTs**, Nikolas Papadopoulos, Florian De Roose, Marc Ameys, Wim Dehaene, Jan Genoe ,Kris Myny, Yi-Cheng Lai, Jan-Laurens van der Steen

Dual-gate InGaZnO TFTs are demonstrated to achieve a 6-bit SAR ADC operated at a clock of 400Hz and a power dissipation of 52.2μW at a supply of 15V on flexible substrate. DNL of 0.7LSB and an INL of 0.58 LSB using only n-type TFTs and FoM of 66.7nJ/c.s. is achieved.

27-2 **Smart-Wire: A 0.5V 44uW 0°C to 100°C Powerline Energy Harvesting Sensor Node**, A. Chua, R. Maestro, J. Jardin, K. Monisit, R. Nuestro, K. Fabay, B. Pelayo, W. Lofamia, J. Ortiz, J. Madamba, L. Alarcon, University of the Philippines-Diliman

A 44µW 0.5V self-powered powerline-monitoring sensor node is implemented in 65nm CMOS. A 450kHz 30kbps BPSK-modulated transceiver enables 1.5-meter node-to-node powerline communication at 10E-6 BER. The node has a 3.354 ENOB 50kSps SAR ADC for current measurements and a 440Sps time-to-digital converter for 0-100°C temperature measurements with 1.12°C granularity.

27-3 **A Monolithically Integrated, Optically Clocked 10GS/s Sampler with a Bandwidth of > 30GHz and a Jitter of < 30fs in Photonic SiGe BiCMOS Technology**, Benjamin Krueger*/****, Robert Elvis Makon∗, Oliver Landolt*, Ols Hidri∗, Thomas Schweiger∗, Edgar Krune**, Dieter Knoll***, Stefan Lischke***, Joerg Schulze****, *Rohde & Schwarz GmbH & Co. KG, Munich, Germany, **Technische Universitaet Berlin, Berlin, G

An optically clocked 10GS/s sampler integrated in a photonic 0.25µm SiGe-BiCMOS technology uses an optical pulse train generated by a mode-locked laser to sample an electrical signal. Experimental results demonstrate a bandwidth >30GHz, a jitter <30fs, a THD <−33dB over the entire bandwidth, and a SNR of 35.3dB.