IEEE CICC Call for Papers

Submission Deadline is November 6, 2017

IEEE Custom Integrated Circuits Conference (CICC)
is sponsored by the IEEE Solid-State Circuits Society
and technically co-sponsored by the IEEE Electron Devices Society

DoubleTree Mission Valley
San Diego, CA
April 8 – April 11, 2018

CICC 2018 welcomes submissions of original and unpublished work on:

Analog Circuits and Techniques for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.

Power Management circuits and design techniques including DC-DC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.

Data Converters of all types enabled by new techniques, architectures, or technologies.

Wireless Transceivers and RF/mm-Wave Circuits for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.

Wireline and Optical Communications Circuits and Systems for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Design Foundations

- High-level system modeling, digital design infrastructure, and mixed-mode (analog-digital) verification for complex SOCs. Novel digital architectures for emerging applications. Design methodologies for functional safety.
- Modeling and simulation of advanced CMOS and power devices to improve design quality, efficiency, and reliability. Design methodologies for emerging applications (deep learning, automobile, IoT, security), and design for manufacture, test, aging and reliability (novel DFT circuits, system-level testing).

Emerging Technologies, Systems, and Applications

Emerging technologies solicit hardware focused papers in the technologies of tomorrow extending from new device and memory technology to system integration, applications and packaging with focus on, but not limited to:

- **Hardware-based artificial intelligence and security.** Hardware designs for emerging algorithms, hardware security, hardware and energy-efficient artificial intelligence, machine learning, deep learning accelerators. Applications include autonomous transportation and cloud computing.
- **Next-generation devices, technology, integration and packaging** including nano-primitives, non-silicon based technology, MEMS, emerging memories, non-traditional circuits, mm-wave/THz passives and integration, flexible, printed, large-area and organic electronics. system in package, 2.5D, 3D and monolithic 3DIC, multi-die heterogeneous integration, silicon photonic interconnects and packaging, advanced assembly and bonding, embedded cooling technologies,
- **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

Conference Technical Sessions and Events

Technical Sessions addressing a broad range of circuits, applications, design techniques, tools, test, reliability, and emerging technologies, and providing education on new, state-of-the-art developments is the core of the CICC technical program.

Educational Sessions instructed by recognized invited speakers who are among the best in the industry are included in the conference. They are valuable opportunities to refresh key skills in traditional circuit-design methods and acquire knowledge in vital new areas in analog, digital, and RF integrated circuit design.

Panels, ***Forums*** and a ***Plenary Session*** provide a platform for leaders from the IC industry and academia to present highlights on new field of research and development related to circuit design and to debate key issues and controversial topics. CICC panels are well known for their lively and thought-provoking discussion and audience participation.

Our ***Exhibit***, is where semiconductor manufacturers, IP providers, SW tool suppliers, design-service houses, and technical book publishers offer of their products. Our ***Welcome Reception***, ***Conference Luncheon*** and ***Exhibit*** with food and beverage, provide additional opportunities for discussion and peer networking.

Paper Submission

Papers may be **3 - 4 pages** in length, be camera-ready and **submitted electronically** in PDF format using the CICC website (www.ieee-cicc.org). Appropriate company and government clearances MUST be obtained prior to submission. Papers must report an **original unpublished work** and concisely explain how the state-of-the-art is advanced, including results. Circuit-design papers must include measured experimental results that substantiate performance claims. Deadline for submission of technical papers is **November 6, 2017**. Authors of accepted papers will be notified by email by **January 16, 2018**. Top-rated papers are also eligible for publication in a special issue of the **IEEE Journal of Solid State Circuits**.

For more information on paper submission, please visit the conference website (www.ieee-cicc.org). On the menu at the top, click on Call for Papers, then Paper Submission.

General Chair
Kimo Tam, *Analog Devices:* kimo.tam@analog.com

Conference Chair
Alessandro Piovaccari, *Silicon Laboratories:* piovac@ieee.org

Technical Program Chair
Hua Wang, *Georgia Institute of Technology*:
hua.wang@ece.gatech.edu