A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-Based 0-1 MASH ADC with Direct Digital Background Nonlinearity Calibration. K. Ragab, N. Sun, The University of Texas at Austin

This paper presents a direct digital background calibration technique to correct nonlinearity errors in VCO-based 0-1 MASH SD ADCs. The proposed technique altogether corrects VCO gain error, nonlinearity, and capacitor mismatch of the residue generating DAC. It improves SNDR of the prototype ADC from 60dB to 73.4dB in 2.5MHz signal bandwidth. The ADC consumes 4.8mW from 1.8V supply in 180nm CMOS. The measured convergence time is only 64ms.
T-9 A 130nm Canary SRAM for SRAM Dynamic Write $V_{min}$ Tracking across Voltage, Frequency, and Temperature Variations. A. Banerjee, J. Breiholz, B. H. Calhoun, University of Virginia

This paper shows the first silicon results of a working 512b canary SRAM using bitline and wordline type reverse assists in a 130nm bulk technology. The 512b canary SRAM has distinct canary failure trends across voltage, frequency, and temperature variations to track an 8kb SRAM’s dynamic write $V_{min}$.

T-10 A Low Energy SRAM-based Physically Uncloneable Function Primitive in 28 nm CMOS. A. Neale, M. Sachdev, University of Waterloo

A 0.6V low energy 64-kb SRAM-based PUF protected with a multi-bit ECC is fabricated in a 28nm LP-CMOS process. Majority voting and data integrity masking is used to reduce the parity-bit overhead by 65% to yield 100% reproducible PUF responses. Measurement results show an average active access energy of 0.045μJ/bit-cycle.

T-11 A 0.4V–1V 0.2A/mm $^{7}$ 70% Efficient 500MHz Fully Integrated Digitally Controlled 3-Level Buck Voltage Regulator with On-Die High Density MIM Capacitor in 22nm Tri-Gate CMOS. Pavan Kumar, Vaibhav A. Vaidya, Harish Krishnamurthy, Stephen Kim, George E. Matthew, Sheldon Weng, Bharani Thiruvengadam, Wayne Proefrock, Krishnan Ravichandran, Vivek De, Intel Corporation

Circuit techniques to reduce inductor size are attractive to increase power density for On-Die Voltage Regulators. This paper presents a 70–72% efficient, 500MHz digitally controlled 3-level Buck VR on 22nm Tri-Gate CMOS with MIM capacitors. The advantages of the 3-level converter for wide range DVFS over traditional solutions are demonstrated.

T-12 A Single-Inductor 7+7 Ratio Reconfigurable Resonant Switched- Capacitor DC-DC Converter with 0.1-to-1.5V Output Voltage Range. Loai G. Salem, Patrick P. Mercier, University of California San Diego

This paper demonstrates the first 7-ratio resonant switched capacitor (SC) converter using only a single inductor, in CMOS. A frequency-scaled-gear-train recursive topology is introduced that enables soft-charging of all flying-capacitors through one inductor at any arbitrary binary ratio. The converter achieves 14.4% efficiency improvement over co-fabricated SC in 0.18µm bulk.

T-13 A 83fps 1080P Resolution 354 mW Silicon Implementation for Computing the Improved Robust Feature in Affine Space. Shouyi Yin, Peng Ouyang, Leibo Liu, Shaojun Wei, Tsinghua University

In comparison with the popular feature algorithms in vision applications, AFFINE-SIFT (ASIFT) achieves the highest robustness in terms of illumination, rotation, and scale in affine space but exhibits high computation complexity. This work proposes three optimization techniques, including reverse based pipelined affine computing, full parallel Gaussian pyramid computing and rotation invariant binary pattern (RIBP) based feature vector computing, to accelerate the computation intensive parts in ASIFT, and design a high efficient pipelined and parallel architecture for the whole ASIFT. Using TSMC 65 nm process, silicon implementation shows that this work achieves the processing speed of 83fps at 1080p (1000 feature points per frame on average) with 200 MHz while dissipating 354 mW. It fully supports the real time processing of high resolution images in vision scenes with strong robustness.


A wide tuning range 60GHz DCO with fine frequency step is presented. Different tuning techniques are combined to achieve 24% tuning range with a fine frequency resolution of 39 kHz. The phase noise at 1 MHz is -95.1dBc/Hz. The FOM of DCO is -186.4dB which is better than recent DCos.

T-15 A Cartesian Feedback-Feedforward Transmitter IC in 130nm CMOS. Sungmin Ock, Hyejeong Song, Ranjit Gharpurey, The University of Texas at Austin

A transmitter architecture based on Cartesian feedback-feedback is described. A Cartesian feedback loop is used to linearize a transmitter and PA, and the error signal is utilized in a feedforward path to further enhance linearity. A proof-of-concept prototype transmitter IC that is used to linearize an external PA is demonstrated in a 130nm CMOS process. The implementation allows for a 8.7 dB ACLR improvement, compared to an open-loop transmitter, for an output power of 16.6 dBm at 2.4 GHz while employing a 16 QAM LTE signal with 1.4 MHz bandwidth.

T-16 A 0.6-V, 30-GHz Six-Phase VCO with Superharmonic Coupling in 32-nm SOI CMOS Technology. Dongseok Shin, Sanjay Raman, Kwang-Jin Koh, Virginia Tech

This paper presents a six-phase VCO using a superharmonic coupling technique. Three VCOs are coupled by an inductive network in their tail nodes to generate six-phase outputs. This network also serves as a tail noise filter in each VCO. Therefore, the proposed six-phase VCO can achieve better phase noise performance than typical multiphase topologies. The proposed VCO is implemented in 32nm SOI CMOS process with core area of 0.6×0.5mm$^2$. The VCO can be tuned from 29.24 GHz to 31.56 GHz, a frequency tuning range of 7.6% at 0.6V supply. With each VCO consuming 1.52 mW DC power (4.56 mW total), the measured phase noise is -128 dBc/Hz at 10 MHz offset when VCO output frequency is 31.43 GHz, resulting in -191 dBc/Hz of FOM.

T-17 A Dual-Tank LC VCO Topology Approaching Towards the Maximum Thermodynamically-Achievable Oscillator FoM. Amir Nikpaik, Abdolreza Nabavi*, Amir Hossein, Masnadi Shirazi, Sudip Shekhar, Shahriar Mirabbasi, University of British Columbia, *Tarbiat Modares University

A dual tank hard-clipping VCO is presented that can approach the maximum thermodynamically achievable oscillator FoM within 3dB. Compared to class-B/C/D/IF oscillators, it is capable of reducing both close-in and far-cut phase noise (PN). A prototype 4.17-to-4.95GHz VCO achieves -97 and -143 dBc/Hz PN at 30kHz and 3MHz offset, respectively.
T-18  A DC-to-12.5Gb/s 4.88mW/Gb/s All-rate CDR with a single LC VCO in 90nm CMOS, J. Yoon, S. Kwon, H. Bae, KAIST

The proposed CDR supports reference-less all-rate operation with static fractional divider and asynchronous phase calibration scheme. And the IC features an automatic loop gain control scheme which adjusts the bandwidth of a CDR automatically in the background for optimum BER performance. The power efficiency of the test chip is 4.88mW/Gb/s.


A 2.2-to-2.8 GHz 6.8 mW Type-I PLL occupies 0.12 mm² in 0.13-μm CMOS and achieves 490 fs(rms) random jitter, -103.4 dBC/Hz in-band phase noise, -65 dBC reference spur, and 2.5 μs lock-time. Lock range is improved using a saturated-PFD, voltage booster and a digital level shifter, and reference spur is suppressed using a S/H envelope detector.