2:00 pm  Introduction


This review focuses on material challenges associated with III-V co-integration with Si for future CMOS. There is a huge volume of literature on this topic as implementation of III-V monolithic integration with Si has been the holy grail for last four decades; targeting a wide range of applications including RF devices, LEDs, lasers, photo-detectors and the like. The key drivers have been the cost reduction, scalability with Si wafer diameter, and accessibility to highly scaled integrated circuits next to III-V devices. With the current focus on CMOS the pace of progress on monolithic integration has accelerated by leaps and bounds partly because of its vast impact on CMOS scaling, and partly due to the aggressive CMOS roadmap requirements. The discussion below concentrates on In$_{0.53}$Ga$_{0.47}$As channel which is the dominant III-V material being pursued for future technology. Despite the narrow focus, fundamental and engineering challenges posed by this material encompass a broad range of material topics including epitaxial growth, crystallographic defects and their dynamics during growth and subsequent processing, clever device architecture to alleviate adverse impact of defects on device leakage, and innovative engineering for material improvement.

2:55 pm  Recent Advances in GaN MMIC Technology (INVITED), N. Kolias, Raytheon Company

GaN MMIC technology is now in production and is revolutionizing microwave systems. In this paper we present an overview of GaN MMIC technology, focusing on device characteristics, reliability, and high frequency performance. We also introduce emerging GaN technologies such as GaN-on-diamond and the heterogeneous integration of GaN with Silicon.

3:20 pm  A Novel Low Cost, High Performance and Reliable Silicon Interposer (INVITED), Farhang Yazdani, BroadPak Corporation

Silicon interposer has emerged as a substrate of choice for integrating fine pitch, high density devices. Conventional packaging of 2.5D/3D devices involves multiple level of assemblies. Normally, 2.5D/3D devices are first assembled on thinned silicon interposer with aspect ratio of 10:100 followed by second level assembly on a multi-layer organic build-up substrate. In this study we introduce direct assembly of silicon interposer on PCB, resulting in reduced cost and increased performance. We investigate effect of under-fill on solder joint reliability during direct assembly of silicon interposer on PCB. A 10x10mm$^2$ interposer test vehicle was designed and fabricated on 310µm thick rigid silicon substrate. BGA of side of the interposer was bumped with eutectic solder balls through a reflow process. Interposer was then assembled on a 50X50mm$^2$ FR-4 PCB through a reflow process. We present cost analysis, design flow, and direct assembly of rigid silicon interposer on PCB. Effect of under-fill on the solder joint reliability is
demonstrated using CSAM images during temperature cycles at 250, 500, 750 and 1000 intervals. It is shown that all samples successfully passed the temperature cycle stress test.


3D technologies offer significant potential to improve performance and performance per unit power. After exploiting TSV technologies for cost reduction and increasing memory bandwidth, the next frontier is to create more sophisticated solutions that promise further increases in performance/power beyond those attributable to memory interfaces alone. These include heterogeneous integration for trusted design and exploitation of the high amounts of interconnect available to provide for customization. Challenges include access for prototype quantities and the design of sophisticated static and dynamic thermal management methods and technologies.