Session 2 - Low Power Analog
Monday Morning, September 28, Oak Ballroom

Session Chair: Shahrazad Naraghi, Tektronix
Session Co-Chair: Alessandro Piovaccari, Silicon Laboratories

This session focuses on low power analog circuits and techniques. Deep nanoscale CMOS designs, oscillators and a temperature sensor are highlights.

10:00 am  Introduction

10:05 am  Scaling Analog Circuits into Deep Nanoscale CMOS: Obstacles and Ways to Overcome Them (INVITED), Peter Kinget, Columbia University, NY, NY

Analog circuits provide the critical interfaces between the digital world inside today's integrated circuits and the physical world. Semiconductor technology scaling driven by 'Moore's Law' has resulted in a phenomenal scaling of the performance of digital processors and memory. Continuing design innovations have enabled the scaling of analog interfaces onto scaled CMOS technologies, even though device scaling is a mixed blessing for the analog designer. This paper reviews the scaling challenges for analog circuits ranging from fundamental to practical challenges. Design strategies are outlined that in principle can overcome the challenges and can help guide the search for new circuit paradigms. Several examples of innovative analog design paradigms are reviewed and the opportunities in highly scaled CMOS technologies are outlined.

10:55 am  A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz, H. Wang, P. P. Mercier, University of California, San Diego

This paper presents a gate-leakage-based Hz-range oscillator that achieves ultra-low-power frequency-stable operation in a small area via a capacitive-discharging architecture. Implemented in a 65 nm CMOS process, the proposed oscillator consumes 51 pW at 2.8 Hz and achieve a frequency variation of 937 ppm/°C from -40 °C to 60 °C.


This paper presents a novel ultra-low-power current-mode relaxation oscillator, which produces a 122kHz digital clock while dissipating 14.4nW at 0.6V. The self-biased frequency-compensated oscillator occupies 0.03mm² in 0.18µm CMOS and achieves a figure of merit of 120pW/kHz, making it one of the most efficient relaxation oscillators reported to date.

11:45 am  A 30.1µm², < ±1.1°C-3σ-Error, 0.4-to-1.0V Temperature Sensor based on Direct Threshold-Voltage Sensing for On-Chip Dense Thermal Monitoring, S. Kim, M. Seok, Columbia University

This paper presents an on-chip temperature sensor circuits that directly sense temperature dependency of threshold voltage. The sensor achieves a compact footprint of 30.1µm², error of <±1.1°C (3σ) across 0-100°C after one point calibration, and voltage scalability down to 0.4V without losing accuracy, making it suitable for on-chip dense thermal-monitoring.