Session 10 - Memory Advancements
Monday Afternoon, September 28, Fir Ballroom

Session Chair: Dinesh Somasekhar, Intel
Session Co-Chair: Jean-Christophe Vial, Intel Mobile Communications

Advances in solutions for memory technologies ranging from DRAM, PCRAM, STTRAM, and SRAM are topics covered in this session.

3:30 pm Introduction

3:35 pm 10-1 Design Considerations of HBM Stacked DRAM and the Memory Architecture Extension (INVITED), Dong Uk Lee, Kang Seol Lee, Yongwoo Lee, Kyung Whan Kim, Jong Ho Kang, Jaejin Lee, Jun Hyun Chun, SK Hynix

Recently, the 3D stacked memory, which is known as HBM (high bandwidth memory), using TSV process has been developed. The stacked memory structure provides increased bandwidth, low power consumption, as well as small form factor. There are many design challenges, such as multi-channel operation, microbump test and TSV connection scan. Various design methodology make it possible to overcome the difficulties in the development of TSV technology. Vertical stacking enables more diverse memory architecture than the flat architecture. The next generation of HBM focuses on not only the bandwidth but also the system performance enhancement by adopting pseudo channel and 8-Hi stacking. The architecture applied to the second generation HBM are introduced in this paper.


Non-resistance read metric with drift resilient nature is enhanced to be suitable for high density memory array with large parasitic time constant. Experimental results for a bank of 2Gb multi-level density are demonstrated with total read latency of 450ns.


Spin Transfer Torque Magnetoresistive RAM (STT MRAM) has uniquely attractive write performance and endurance characteristics. Nonetheless, little STT MRAM circuit hardware data has been published. This paper describes a fully-functional 90nm 8Mb STT MRAM, identifies and describes solutions to the primary circuit challenges, and includes considerable circuit hardware data.


This paper presents 64-kb 8T three-port image memory using a 28-nm FD-SOI process technology. In the test chip, the energy minimum point is a supply voltage of 0.54V at a frequency of 18.2MHz, at which 298-fJ/cycle in a write operation and 650-fJ/cycle in a read operation are achieved.