Session 22 - High Frequency Analog Techniques

Wednesday, September 30

Wednesday Morning, September 30, Oak Ballroom

Session Chair: Tim Hancock, Massachusetts Inst. of Tech.
Session Co-Chair: Jorge Grilo, Maxlinear

This session will present analog techniques applied at high frequencies. For tunable filters, a PLL and track-and-hold amplifier.

9:00 am Introduction

9:05 am 22-1

A 4.6mW, 22dBm IIP3 all MOSCAP Based 34-314MHz Tunable Continuous Time Filter in 65nm, Rakesh Kumar Palani, Ramesh Harjani, University of Minnesota

An inverter based filter design is proposed that uses only MOSCAPs as filter capacitors. A 3rd order 34-314 MHz tunable continuous time filter is fabricated in TSMC's 65nm technology. The filter achieves an OIP3 of +25.24 dBm while drawing 4.2mA from a 1.1V supply and occupies an area of 0.007 mm².

9:30 am 22-2

2.4 GHz Q-Tunable LC Bandpass Filter with 172-dBxHz Peak Dynamic Range, Resilient to +15-dBm Out-of-Band Blocker, Laya Mohammadi, Kwang-Jin Koh, Virginia Tech

This paper presents a new Q-enhancement LC bandpass filter capable of 2.25~4.5 GHz frequency tuning range with independent Q control from 3 to 150. A dual varactor inverse (DVI) control method is proposed to suppress varactor nonlinearity. Also, the BPF employs a dynamic negative resistance circuit that introduces a gain peaking when the filter output reaches 1-dB gain compression point, extending the P-1dB input power. The circuit is implemented in a 0.13 μm SiGe BiCMOS process. Measurement results show 9~8 dBm of maximum IP-1dB, 10~18.5 dB of minimum NF, resulting in 147-172 dBxHz of normalized dynamic range when Q varies from 3 to 150. The BPF consumes 13-20 mA from 3.3 V supply. Chip size is 0.63×0.63 mm².

9:55 am 22-3

An Injection Locked PLL for Power Supply Variation Robustness Using Negative Phase Shift Phenomenon of Injection Locked Frequency Divider, Dongil Lee, Taeho Lee, Yong-Hun Kim, Young-Ju Kim, Lee-Sup Kim, KAIST

This paper presents a 2 GHz injection-locked PLL (ILPLL) with an injection-locked frequency divider (ILFD). Using a negative phase shift phenomenon of the ILFD, injection timing can be calibrated without a delay line. As a result, the proposed ILPLL achieves a simple background injection timing calibration for robustness of power supply variation. The test core has been fabricated in 65nm CMOS process consuming 3.74mW at 0.9V supply voltage.

10:20 am 22-4

A 200-MS/s 98-dB SNR Track-and-Hold in 0.25-μm GaN HEMT, S. Chung*, H.-S. Lee, Massachusetts Institute of Technology, *University of Southern California

In order to overcome the design challenges of GaN HEMT leakage and Schottky diode turn-on, a GaN track-and-hold (T/H) circuit with 20-V pseudo-differential input swing consists of an asymmetric gate device followed by a symmetric gate device. The GaN T/H provides 98-dB SNR at 200 MS/s while drawing 195 mA.

10:45 am Break

Session 23 - Modeling Emerging Devices

Wednesday, September 30

Wednesday Morning, September 30, Fir Ballroom

Session Chair: Chenjie Gu, Intel
Session Co-Chair: Hidetoshi Onodera, Kyoto University

This session presents compact models for emerging “More-than-Moore” devices as well as modeling and statistical techniques accounting for device variability.

9:00 am Introduction

9:05 am 23-1

Physics-based Compact Models for Insulated-Gate Field-Effect Biosensors, Landau-Transistors, and Thin-Film Solar Cells (INVITED), M. A. Alam, P. Dak, M. A. Wahab, X. Sun, Purdue University, West Lafayette

As the future of Moore’s law appear uncertain, semiconductor electronics is being reinvented with a broader focus on energy efficient 3D computing, flexible electronics, biosensors, energy harvesting, etc. These devices are gradually being integrated onto the CMOS fabric as ‘More-than-Moore’ components, with transformative impact on consumer
The development of a scalable and user-friendly SPICE model is a key aspect of exploring the potential of spin-transfer torque MRAM (STT-MRAM). A self-contained magnetic tunnel junction (MTJ) SPICE model is proposed in this work which can reproduce realistic MTJ characteristics based on user-defined input parameters such as the free layer’s length, width, and thickness. Using the propose model, scalability studies of both in-plane and perpendicular MTJs can be performed across different technology nodes with minimal effort, which differentiates this model from most previously reported models.

The drain current of a multi-finger MOSFET is typically calculated as the product of that of a single-finger MOSFET and the number of fingers. Careful investigation of currents in different fingers of a multi-finger transistor in the presence of parasitic effects shows differences between the per-finger drain current of the multi-finger transistor and the drain current of a corresponding single-finger transistor. We show that each of the following factors alone causes the drain current in one or more fingers of a multi-finger transistor to be different from that in other fingers of the transistor and the per-finger drain current of the multi-finger transistor to be different from the drain current of a corresponding single-finger transistor: (a) the resistance of wires that connect multiple fingers together, (b) the contact resistance, (c) the diffusion resistance, and (d) self heating. Excluding all of the above factors, the uncorrelated variations among the sub-threshold drain currents of different finger cause the per-finger median sub-threshold drain current of the multi-finger transistor to be different from the median sub-threshold drain current of the single-finger transistor.

In this paper, we propose a novel Bayesian scaled-sigma sampling (BSSS) technique to analyze the rare failure events of nanoscale ICs in a high-dimensional space. An SRAM sense amplifier example designed in a 45 nm CMOS process is used to demonstrate the efficacy of BSSS.
demonstrated to radiate pulse trains of 2.6ps time-widths, pure tones at 107.5GHz, 215GHz and any combination of these two harmonic frequencies.

10:20 am Advanced Wireless Power and Data Transmission Techniques for Implantable Medical Devices (INVITED), H.-M. Lee, M.Kiani*, M. Ghovanloo**, Massachusetts Institute of Technology, *Pennsylvania State University, **Georgia Institute of Technology

This paper reviews various mechanisms for wireless power transmission with focus on efficient link structures and circuit techniques for implantable medical devices. These devices also require wireless data telemetry for wideband bidirectional data communication in the presence of the strong power carrier interference. This paper discusses several modulation schemes and transceiver circuits for low-power, carrier-less, and robust wireless data transmission.

10:45 am Break

Session 25 - 20 Gb/s Transmitters and Receivers

Wednesday Morning, September 30, Oak Ballroom

Session Chair: Jun Cao, Broadcom
Session Co-Chair: Shahriar Mirabbasi, University of British Columbia

This session presents innovative techniques for low-power 20 Gb/s optical and electrical transmitters and receivers.

11:00 am Introduction

11:05 am A 20 Gb/s 0.3 pJ/b Singe-Ended Die-to-Die Transceiver in 28 nm-SOI CMOS, B. Dehlaghi, A. C. Carusone, University of Toronto

A low-power transceiver architecture for die-to-die applications is presented. The proposed transceiver employs CMOS logic-style circuits and a passive equalizer in the transmitter to reduce the power consumption. Single-ended signaling without a shared reference voltage is used to minimize the number of required signal traces and packaging bumps. A transceiver prototype is fabricated in 28 nm STM FD-SOI CMOS technology and it operates at 20 Gb/s and 16.4 Gb/s data rates over different channels with 5.9 and 7.1 dB of loss relative to DC (10.7 and 12.9 dB total loss) at the Nyquist frequency while consuming 0.30 and 0.33 pJ/bit excluding clocking circuits, respectively.


A 4×20Gb/s SST transmitter with 2-tap FFE and FEXT cancellation is presented. The FFE and XTC are merged together with the SST driver. The proposed divider-less clock generation saves much power. Fabricated in 65nm CMOS, the transmitter achieves a maximum data rate of 20Gb/s with a power efficiency of 0.86pJ/blane.

11:50 am A 20Gb/s 0.77pJ/bl VCSEL Transmitter with Nonlinear Equalization in 32nm SOI CMOS, Mayank Raj, Manuel Monge, Azita Emami, California Institute of Technology

This paper describes an ultra-low-power VCSEL transmitter in 32nm SOI CMOS. To increase its power efficiency, the VCSEL is driven at a low bias current. The resulting nonlinearity and loss in bandwidth is modelled and compensated by a nonlinear equalization technique that achieves 0.77pJ/bl power efficiency at 20Gb/s.

Educational Session 7

Wednesday Morning, September 30, Cedar Ballroom

Session Chair: John McNeill, Worcester Polytechnic Institute
Session Co-Chair: Mohammad Ranjbar, Inphi Corporation

9:00 am SAR ADCs in time-interleaved converter arrays, Ron Kapusta, Analog Devices

The time-interleaved ADC was first published more than 30 years ago, yet recently has experienced a surge in interest, as the demand for increased bandwidth has outstripped the performance capability of existing single-core ADCs. Concurrent with this trend has been recent focus on the SAR ADC architecture. As it turns out, the SAR ADC is particularly well-suited for use in time-interleaved arrays. This tutorial talk will review the use of highly-parallel and time-interleaved converter arrays, including both the benefits provided to and the additional constraints placed upon the system. Similarly, the SAR architecture will be examined, demonstrating how its trade-offs, as compared to other
ADC architectures, interact almost synergistically with the time-interleaved configuration. Finally, a number of case studies will be presented to highlight some recent advances in achieving very high data throughput while maintaining the required accuracy. Enabling design and calibration techniques will be covered.

Ron Kapusta received the B. S. and M. Eng. degrees from the Massachusetts Institute of Technology, in 2001. Upon graduation, he joined Analog Devices, designing data converters and sensor interface circuits for multiple channel data acquisition systems. More recently, he has been with the Automotive Technology group, working on signal acquisition for MEMS-based inertial systems. Ron has presented at multiple IEEE conferences in addition to journal papers. He holds more than 40 U.S. and international patents and won the 2013 JSSC Best Paper award. He has served on the technical program committees for CICC and VLSI Circuits.

10:30 am Break

Session 26 - Forum- Advanced Power Amplifier Techniques for Mobile Devices

Wednesday Afternoon, September 30, Oak Ballroom

Organizers:
Yanjie Wang (Intel)
Debopriyo Chowdhury (Broadcom)

The focus of this forum is on how to exploiting impedance transformation techniques in integrated CMOS Power Amplifiers for average power efficiency boosting. Impedance modulation is a powerful technique that can help boost efficiency at lower average power levels for power amplifier and can even be extended to wideband signals. We are going to explore suitable and efficient methods of achieving impedance transformation in CMOS integrated power amplifiers - which can enhance average efficiency, thereby improving overall battery life in portable applications.

1:30 pm A Dual Mode Transformer-Coupled CMOS Class AB Power Amplifier with Back-Off Efficiency Enhancement, Debopriyo Chowdhury (Broadcom Corporation)
Leveraging RF Power DACs to Enhance the Doherty Power Amplifier and Broadband Power Amplifier, Hua Wang (Georgia Tech)
mm-Wave Digital Power Amplifier with Dynamic Load Modulation, Eric Kerherve (University of Bordeaux)
Power Efficient PA matching design on Advanced CMOS Technology, Hongtao Xu (Fudan University, Shanghai, China)
Switched Capacitor RFDACs For Power Efficient Multimode Transmitter, Michael Fulde (Intel)

Educational Session 8

Wednesday Afternoon, September 30, Cedar Ballroom

Session Chair: Jay Wang
Session Co-Chair: Byunghoo Jung

1:30 pm Resonant Wireless Power Transfer: Technology and Integration Roadmap, Francesco Carobolante, Qualcomm

The promise of Resonant Wireless Power Transfer to enable seamless user experience while charging a variety of mobile devices with differing power requirements (from wearable and mobile devices to tablets and notebooks) is finally reaching maturity. While the specifications are now available and hardware is shown to be capable of charging devices from less than 1W up to 50W, the process of integration is now on the way, in order to address coexistence of the technology with the rest of the system, as well as size and cost constraints. After an introduction to Magnetic Resonance Wireless Power Transfer technology, this presentation will provide an overview of the challenges and trade-offs that led to the development of its specifications (including frequency selection, efficiency and thermal requirements, and other regulatory and use case considerations). Circuit implementations for both Transmitter and Receiver will be introduced, with a focus on new silicon and packaging technologies that enable high levels of integration, especially in space-constrained wearable devices and high power applications like notebooks.

Francesco Carobolante is Vice President of Engineering at Qualcomm Incorporated. In this position, he has been responsible for the development of products and technologies for mixed signal Integrated Circuits (primarily in Power Management and analog subsystems). He is currently leading the development of Wireless Power Transfer technology and its standardization through A4WP (the Alliance for Wireless Power). Prior to joining Qualcomm, he held positions at STMicroelectronics, Tripath Technology and Fairchild Semiconductors, developing analog, power, and MEMS based mixed signal products. He holds more than 50 patents and has published several papers on power, mixed signal and system design. He received an Electrical Engineering and PE degrees from the University of Padova in Italy, and a MSEE from UCLA.