Technical Sessions

Mon., Sept. 28 – Wed., Sept. 30

Session 1 - Plenary Session
Monday Morning, September 28, Oak Ballroom

Session Chair: Kimo Tam, Analog Devices

8:00 am Welcome and Opening Remarks
Award Presentations
Keynote Speaker Introduction

Keynote Presentation
Dr. Fari Assaderaghi is Vice President of Advanced Technology Development at InvenSense.

Smart Low-Power MEMS Help Usher in the Wearable Era
Wearable devices are finally transitioning from hype to mainstream, aided by integration of valuable transducers, identification of application and use cases, ramp up of cloud services, and increased public awareness and interest due to Apple’s watch introduction. Although still a nascent field, several themes are emerging:

The wrist is only one of many targets for these devices. Smart glasses, hearables (ear as a natural place and rich with health information), necklaces, finger and hip worn products, and smart clothes are all becoming realities. Due to severe size constraints, several new user interfaces, such as audio, are becoming critical.

Wearables are evolving from ability to perform simple functions such as step count, to becoming contextually aware products, providing richer user experience and data (health, fitness, infotainment, IoT control). These capabilities are in turn enabled by a plethora of transducers such as accelerometers, gyroscopes, magnetometers, pressure sensors, haptics, and microphones. Many new sensors and actuators are emerging:

Due to the desire for “always on” capability, small size limit, and appeal of charging only every few days, power is one of the most important parameters impacting the entire system design. Innovative circuit techniques target extreme low power. Smart combo sensors (MEMS SOC) handle tasks locally on chip instead of sending raw data to processor/cloud. Dedicated algorithms and software running on these smart combo sensors further reduce the system power (e.g. run-time calibration, streaming/batching of data, automatic activity recognition, heavy duty cycling of power-hungry functions such as GNSS). Finally, low-power wireless links enable connectivity of wearables to smart phones and other devices, and eventually to the cloud.

Session 2 - Low Power Analog
Monday Morning, September 28, Oak Ballroom

Session Chair: Shahrzad Naraghi, Tectronix
Session Co-Chair: Alessandro Piovaccari, Silicon Laboratories

This session focuses on low power analog circuits and techniques. Deep nanoscale CMOS designs, oscillators and a temperature sensor are highlights.

10:00 am Introduction

10:05 am 2-1 Scaling Analog Circuits into Deep Nanoscale CMOS: Obstacles and Ways to Overcome Them (INVITED), Peter Kinget, Columbia University, NY, NY

Analog circuits provide the critical interfaces between the digital world inside today’s integrated circuits and the physical world. Semiconductor technology scaling driven by Moore’s Law has resulted in a phenomenal scaling of the performance of digital processors and memory. Continuing design innovations have enabled the scaling of analog interfaces onto scaled CMOS technologies, even though device scaling is a mixed blessing for the analog designer. This paper reviews the scaling challenges for analog circuits ranging from fundamental to practical challenges. Design strategies are outlined that in principle can overcome the challenges and can help guide the search for new circuit paradigms. Several examples of innovative analog design paradigms are reviewed and the opportunities in highly scaled CMOS technologies are outlined.

10:55 am 2-2 A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz, H. Wang, P. P. Mercier, University of California, San Diego

This paper presents a gate-leakage-based Hz-range oscillator that achieves ultra-low-power frequency-stable operation in a small area via a capacitive-discharging architecture. Implemented in a 65 nm CMOS process, the proposed oscillator consumes 51 pW at 2.8 Hz and achieve a frequency variation of 937 ppm/°C from -40 °C to 60 °C.
Session 3 - Optical Interconnect and Reliability Enhancement Techniques

Monday Morning, September 28, Fir Ballroom

Session Chair: Tetsuya Iizuka, Univ. of Tokyo
Session Co-Chair: Takahiro Yamaguchi, Advantest Laboratories Ltd

This session presents state-of-the-art electrical and optical concurrent design techniques for optical interconnect as well as reliability enhancement approaches for device aging.

10:00 am  Introduction

10:05 am  An Electrical and Optical Concurrent Design Methodology for Enlarging Jitter Margin of 25.8-Gb/s Optical Interconnects (INVITED), Takashi Takemoto, Hiroki Yamashita, Yasunobu Matsuoka, Yong Lee, and Masaru Kokubo, Hitachi, Ltd.

An electrical and optical concurrent design methodology for maximizing jitter margin of optical transmissions between FPGAs is established. As a key for establishing it, a method for modeling jitter of a LD based on measured rising/falling step responses is proposed. Optimizing equalization gain experimentally achieved 25.8-Gb/s error-free optical transmission.

10:55 am  Circuit Techniques for Mitigating Short-Term Vth Instability Issues in Successive Approximation Register (SAR) ADCs, Won Ho Choi, Hoonki Kim, and Chris H. Kim, University of Minnesota

Stress equalization and stress removal techniques for mitigating short-term Vth instability issues in SAR ADCs have been experimentally verified using an 80kS/s 10-bit differential SAR ADC fabricated in a 65nm LP CMOS process. The proposed techniques are particularly effective in enhancing the performance of high resolution and low sample rate SAR ADCs which are known to be more susceptible to short-term Vth degradation and recovery effects induced by Bias Temperature Instability (BTI). Experimental data shows that the proposed techniques can reduce the worst case DNL by 0.90 LSB and 0.77 LSB, respectively, compared to a typical SAR ADC.

11:20 am  Timing in-situ monitors: implementation strategy and applications results, A. Benhassain1,2, F. Cacho1, V. Huard1, M. Saliva1,2, L. Anghel3, C. Parthasarathy1, A. Jain1, F. Giner1, 1STMicroelectronics,2 Grenoble university

In this paper, we demonstrate that the usage of in-situ monitors with a feedback loop of voltage regulation is suitable for process compensation, multiples OPP modes, temperature and ageing compensation.

11:45 am  Aging-Aware Adaptive Voltage Scaling in 22nm High-K/Metal-Gate Tri-Gate CMOS, Minki Cho, Carlos Tokunaga, Muhammad M. Khellah, James W. Tschanz, Vivek De, Circuit Research Lab, Intel labs, Hillsboro, OR

Aging-aware Adaptive Voltage Scaling (AVS) can eliminate conventional flat voltage guard band typically added to intrinsic chip VCC to account for transistor aging, therefore reducing power consumption throughout the lifetime of the chip. Aging-aware AVS applied to a Tunable Replica Circuit (TRC) built in a 22nm test chip demonstrates a measured power reduction of a maximum of ~7% at beginning of life and a minimum of ~2% at end of life.

Session 4 - Frequency and Phase Generation Techniques

Monday Morning, September 28, Pine Ballroom

Session Chair: Fa Foster Dai, Auburn University
Session Co-Chair: Swaminathan Sankaran, Texas Instruments
This session presents techniques for frequency locking and schemes for interpolated phase generation with full 2π coverage at RF/mmWave frequencies.

<table>
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<tr>
<th>Time</th>
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<tr>
<td>10:00 am</td>
<td><strong>Introduction</strong></td>
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<td>10:05 am</td>
<td><strong>Sub-Sampling PLL Techniques (INVITED)</strong>, Xiang Gao, Eric Klumperink*, Bram Nauta* Marvell, Santa Clara, CA, *University of Twente, Enschede, Netherlands</td>
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<td>In a classical PLL, the phase detector (PD) and charge pump (CP) noise is multiplied by N², when referred to the VCO output, due to the divide-by-N in the feedback path. It often dominates the in-band phase noise and limits the achievable PLL jitter-power Figure-Of-Merit (FOM). A sub-sampling PLL uses a PD that sub-samples the high frequency VCO output with the reference clock. The PD and CP noise in this PLL is shown to be not multiplied by N², and greatly attenuated by the high phase detection gain, leading to lower in-band phase noise and better PLL FOM. This article reviews the development of the PLL FOM, the sub-sampling PLL techniques and their applications in recent PLL architectures.</td>
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<td>10:55 am</td>
<td><strong>A 2.24GHz 360° Full-Span Differential Vector Modulator Phase Rotator with Transformer-Based Poly-Phase Quadrature Network</strong>, T. W. Li, J. S. Park, H. Wang, Georgia Institute of Technology</td>
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<td>This paper presents a differential vector modulator phase rotator performing 360° full span phase interpolation over a first-ever decade-wide instantaneous bandwidth (2GHz-24GHz). A wideband poly-phase network based on folded transformer 90° couplers generates accurate differential quadrature signals with low passive loss (2dB) over a decade bandwidth. Two 5-bit linear digital variable gain amplifiers (VGAs) scale the quadrature signals, which are then combined for the target phase interpolations. Our phase rotator occupies a very compact chip size (1.2mm-by-1.8mm) in a standard 65nm CMOS process. Moreover, our design does not require any tuning element, band selection switch, or frequency-dependent code compensation/look-up table, ensuring that each phase interpolation code can be used for all the in-band operation frequencies. Additionally, the maximum RMS quantization phase error is only 1.22° within 1.5dB output magnitude variation for full 360° interpolation from 2GHz to 24GHz.</td>
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<td>11:20 am</td>
<td><strong>A 3.9 mW, 35-44/41-59.5 GHz Distributed Injection Locked Frequency Divider</strong>, Alireza Imani, Hossein Hashemi, University of Southern California</td>
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<td>Distributed injection-locked frequency division concept, principle, and design methodology at mm-wave frequencies are presented. A proof-of-concept prototype, realized in a foundry 130 nm BiCMOS SiGe HBT technology, achieves a measured locking range of 35-44 GHz and 41-59.5 GHz while consuming 3.9 mW from a 1.1 V supply.</td>
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<td>11:45 am</td>
<td><strong>A Millimeter-Wave Fully Differential Transformer-Based Passive Reflective-Type Phase Shifter</strong>, T. W. Li, H. Wang, Georgia Institute of Technology</td>
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<td>This paper presents a millimeter-wave fully differential compact transformer-based passive reflective-type phase shifter (RTPS). The proposed RTPS design employs two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads, offering low-loss and an ultra-compact chip size. A proof-of-concept design at 62GHz is implemented in a standard 130nm BiCMOS process with a core area of 340μm-by-340μm. It achieves a wide phase shifting range (up to 367°) and a low insertion loss (IL) (3.7dB&lt;</td>
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Monday Morning, September 28, Cedar Ballroom

Session Chair: Tim Hancock, Massachusetts Institute of Technology
Session Co-Chair: Eric Naviasky, Cadence Design

10:00 am  | **Low Dropout Regulators**, Pavan Hanumolu, University of Illinois, Urbana-Champaign |
|           | This tutorial presents the design, analysis, and practical circuit implementation of low dropout regulators (LDOs). We begin with a review of traditional LDO regulator topologies and evaluate their key performance metrics such as dropout voltage, power supply rejection ratio, load and line regulation accuracy, settling time in the presence of load step, current efficiency, and stability. Following this, we describe alternate LDO architectures and illustrate how one can tradeoff some of the aforementioned performance metrics. We conclude with case study of a few state-of-the-art high performance LDOs. Pavan Hanumolu is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, in 2006, where he subsequently served as a faculty member till 2013. Dr. Hanumolu’s research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion. |
Session 5 - Panel

Monday Afternoon, September 28, Oak Ballroom

1:30 pm  Impedance Mismatch between Academia and Industry

Organizers:
Ayman Shabra, Masdar Institute of Science and Technology
Manoj Sachdev, Univ. of Waterloo

Panelists:
Elad Alon (Uni. Of California, Berkeley)
George Chien (MediaTek)
Peter Kinget (Colombia University)
Seyfi Bazarjani (Qualcomm)
Terri Fiez (Oregon State University)

This panel will explore to what extent should the training of graduate students enable their easy integration into today’s workforce. The very nature of long-term and predominately government sponsored research can create an impedance mismatch between industry and academia especially given the current stage of the lifecycle of the semiconductor industry. It will not be surprising if students learn fundamentals and skills that do not match the immediate needs of industry when they graduate. What is the extent of this mismatch and should we do something about it?

Session 6 - Analog Circuits Using Digital Cells

Monday Afternoon, September 28, Fir Ballroom

Session Chair: Jing Yang, Texas Instruments
Session Co-Chair: Arijit Raychowdhury, Georgia Institute of Technology

Analog circuits have been facilitated by digital cells. Technology of inverter based, ring oscillator based and standard digital cells are used to design the analog functions.

1:30 pm  Introduction

1:35 pm  6-1 Design of PVT Tolerant Inverter Based Circuits for Low Supply Voltages (INVITED), Ramesh Harjani, Rakesh Kumar Palani, University of Minnesota

In this paper, we discuss traditional amplifiers and why inverter based amplifiers are better suited for lower supplies. We then describe the design procedure for inverter based OTA designs with an emphasis on PVT tolerant biasing. We finally validate our designs using measurement results.

2:25 pm  6-2 An 8bit, 2.6ps Two-Step TDC in 65nm CMOS Employing a Switched Ring-Oscillator Based Time Amplifier, B. Kim, H. Kim*, C. H. Kim*, Rambus Inc., *University of Minnesota

An 8bit two-step time-to-digital converter (TDC) with a novel digital switched ring-oscillator based time amplifier (TA) is demonstrated in 65nm CMOS. The proposed TA achieves a predictable and programmable gain without requiring any calibration. The implemented 8bit two-step TDC with a 16x TA gain achieves a time resolution of 2.6ps at 80MS/s conversion rate while consuming 2mW. The measured DNL and INL are 1.84LSB and 2.36LSB, respectively. The TDC area is 0.07mm².

2:50 pm  6-3 A Fully Synthesized 0.4V 77dB SFDR Reprogrammable SRMC Filter Using Digital Standard Cells, Jun Liu, Ahmed Fahmy, Taewook Kim, Nima Maghari, University of Florida

This paper presents a fully synthesized 0.4V analog Biquad filter in a 0.13µm technology using digital standard cells. A new fully reprogrammable multi-stage opamp array is introduced which can provide variable gain and bandwidth depending on the desired performance. In the proposed analog filter, all the active blocks such as the opamps and matched-RC duty-cycle generator are implemented using digital gates. This filter is implemented using Verilog code and synthesized using automated place and route. The prototype IC achieves 77.17dB peak SFDR and a tunable bandwidth of 1.7-2.5MHz while consuming 0.8mW power from a 0.4V analog supply and 1V supply for the switches.

3:15 pm  Break
Session 7 - Advances in Biomedical Sensor Systems

Monday Afternoon, September 28, Pine Ballroom

Session Chair: Christophe Antoine, Analog Devices
Session Co-Chair: Rikky Muller, Coretera Neurotechnologies

This session covers the latest advances in sensing, processing, power management and bidirectional telemetry for biomedical sensor systems.

1:30 pm Introduction

1:35 pm
7-1 A 201mV/pH, 375 fps and 512x576 CMOS ISFET Sensor in 65nm CMOS Technology, Y. Jiang, X. Liu, X. Huang, J. Guo, M. Yan, H. Yu, J.C. Huang*, C.H. Hsieh*, T.T. Chen*, Nanyang Technological University,*TSMC

A 512x576 ISFET array is fabricated in CMOS 65nm process with high-gain (201mV/pH) readout by pH-to-voltage conversion and also with fast readout speed of 375 fps, towards DNA sequencing.

2:00 pm
7-2 A Voltage Doubling Passive Rectifier/Regulator Circuit for Biomedical Implants, Edward Lee, Alfred Mann Foundation

A circuit called prectulator is proposed in this paper. It utilizes the output transistor (MPR) of a linear regulator also as a passive rectifier for providing a regulated DC output from an AC input. The bulk voltage and the gate voltage (VG) of MPR are biased by an auxiliary rectifier and an error amplifier (AE), respectively. During startup and overload situations, overdriving MPR may occur and is prevented by limiting VG inside AE. Using this technique, a voltage doubling prectulator was implemented in a 0.18µm CMOS process. At 15MHz with a peak AC voltage of 3.6V, a power efficient of 87.7% and a voltage conversion ratio of 1.67 were achieved for a 6V output with a load power of 48.8mW.

2:25 pm

Reconstructing signals accurately is a critical aspect of compressed sensing. We propose a compressed-sensing sensor-on-chip that compresses and also extracts key statistics of the input signal at sampling time. These statistics can be used at the receiver to significantly improve the accuracy of reconstruction. When compared against a conventional compressed-sensing system, our experimental measured results demonstrate an improvement of as much as 9-18 dB in the signal-to-error (SER) of the reconstructed signal, depending on input data type and compression factor.

2:50 pm
7-4 A Full-Duplex Wireless Integrated Transceiver for Implant-to-Air Data Communications, S. Abdollah Mirbozorgi, Hadi Bahrami, Mohamad Sawan, Leslie Rusch, Benoit Gosselin, Laval University

A novel fully-integrated, full-duplex transceiver is presented. Unique features are: 1) RX and TX share the same antenna for minimum size, 2) dual band, RX uses a 2.4-GHz receiver for a 100-Mbps downlink, TX uses IR-UWB for a 500-Mbps uplink (10.8-pJ/b), and 3) size reduced by avoid using circulators/diplexers.

3:15 pm Break

Session 8 - Forum - Silicon Photonics Opportunities and Challenges

Monday Afternoon, September 28, Silicon Valley Ballroom

Organizer: Dr. Mike Peng Li, Altera

This forum reviews the advancements in the past 1-2 years in silicon photonics and optical phase array ICs, as well as a forward looking discussion on quantum dot laser and silicon photonics. Key subjects covered includes: energy efficiency, modulation format, performance, density, testability, manufacturability, and reliability, and applications.

1:00 pm
Recent developments in Heterogeneously Integrated Photonics: Enabling the transformation of photonics from boutique to consumer-scale deployments, John Bowers (UCSB) and Alex Fang (Aurrion)

Impact of Quantum Dot Lasers on Silicon Photonics, Yasuhiko Arakawa (Tokyo University, Japan)

Monolithic Optical Phased Array Transceiver in Commercial Foundry CMOS SOI Process, Hossein Hashemi (USC)

Silicon Photonics in Mainstream Applications, Brian Welch (Luxtera)
Behavioral Modeling Options For Balancing Verification Coverage and Credibility, Jess Chen, Qualcomm

The purpose of verification is to reduce the risk of silicon not meeting performance specifications or worse yet, not functioning. Since the silicon does not yet exist, verification depends on simulations. Simulations in turn depend on models. In verification terms, the classical modeling tradeoff between speed and accuracy translates into a tradeoff between test coverage and model credibility (or validity). Transistor-level models produce the most credible simulations but slow run times and convergence problems severely limit test coverage. At the other extreme, a high level flat model quickly simulates all required tests but is least credible because the high level of abstraction greatly increases the chances for un-modeled circuit bugs and other relevant omitted behaviors. A “good” modeling boundary balances coverage and credibility. The balance is subjective because it depends on schedule, available resources, and acceptable risk. Given how strongly verification depends on the overall modeling strategy, it helps to have as many modeling options as possible. This tutorial describes a few modeling methods to balance coverage and credibility.

Jess Chen manages two groups of radio verification engineers at Qualcomm. Besides his relatively recent managerial duties, Jess has spent the last 20 years modeling RF systems and components at various companies. Before that, he spent 15 years at Lockheed Martin modeling and analyzing space craft power systems, motor drives, and unusual test equipment. Jess earned a BA in physics and applied math from UC Berkeley in 1977, an MS in EE from UC Berkeley in 1982, the degree of engineer in control theory from Stanford University in 1985, and an MS in EE from Santa Clara University in 1991.

Introduction

MAPP: The Berkeley Model and Algorithm Prototyping Platform (INVITED), T. Wang, A. V. Karthik, B. Wu, J. Yao and J. Roychowdhury, University of California, Berkeley

We present the Berkeley Model and Algorithm Prototyping Platform (MAPP), a MATLAB-based framework for conveniently and quickly prototyping device compact models and simulation algorithms. MAPP’s internal code structuring, which differs markedly from that of Berkeley SPICE and related simulators, allows users to add new devices with only minimal knowledge of simulation algorithms, and vice-versa. We describe MAPP’s structuring and provide an overview of its capabilities. MAPP is available as open source under the GNU Public License.

A System-Verilog Behavioral Model for PLLs for Pre-Silicon Validation and Top-Down Design Methodology, A. Lotfy, S. Farooq, Q. Wang, S. Yaldiz, P. Mosalikanti, N. Kurd, Intel Corporation

A System-Verilog behavioral model for charge-pump PLLs based on piece-wise constant real number modeling and table lookup is presented. The proposed model exploits the sampled nature of the PLL where most of its analog behavior takes effect during phase detection. The model simulation run time takes only 1 second. Compared to transistor-level Spice simulations, the model shows a correlation of more than 97%. The PLL model is used to exercise critical features like spread-spectrum clocking and adaptive frequency system. In addition, the model was integrated in a pre-silicon validation environment and enabled catching design bugs.

A Mixed-Domain Modeling Method For RF Systems, Zhimiao Chen, Zhixing Liu, Lei Liao, Ralf Wunderlich, Stefan Heinen, RWTH Aachen

This tutorial describes a few modeling methods to balance coverage and credibility.

Session Chair: Larry Nagel
Session Co-Chair: Larry Clark

Monday Afternoon, September 28, Cedar Ballroom

1:30 pm Behavioral Modeling Options For Balancing Verification Coverage and Credibility, Jess Chen, Qualcomm

The purpose of verification is to reduce the risk of silicon not meeting performance specifications or worse yet, not functioning. Since the silicon does not yet exist, verification depends on simulations. Simulations in turn depend on models. In verification terms, the classical modeling tradeoff between speed and accuracy translates into a tradeoff between test coverage and model credibility (or validity). Transistor-level models produce the most credible simulations but slow run times and convergence problems severely limit test coverage. At the other extreme, a high level flat model quickly simulates all required tests but is least credible because the high level of abstraction greatly increases the chances for un-modeled circuit bugs and other relevant omitted behaviors. A “good” modeling boundary balances coverage and credibility. The balance is subjective because it depends on schedule, available resources, and acceptable risk. Given how strongly verification depends on the overall modeling strategy, it helps to have as many modeling options as possible. This tutorial describes a few modeling methods to balance coverage and credibility.

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3:15 pm Break

Session Chair: Larry Nagel, Omega Enterprises Consulting
Session Co-Chair: Colin McAndrew, Freescale Semiconductor, Inc.

Monday Afternoon, September 28, Oak Ballroom

This session presents new methods for enhanced simulation techniques. The invited paper on this session describes the MAPP Platform from UC Berkeley.

3:30 pm Introduction

3:35 pm MAPP: The Berkeley Model and Algorithm Prototyping Platform (INVITED), T. Wang, A. V. Karthik, B. Wu, J. Yao and J. Roychowdhury, University of California, Berkeley

We present the Berkeley Model and Algorithm Prototyping Platform (MAPP), a MATLAB-based framework for conveniently and quickly prototyping device compact models and simulation algorithms. MAPP’s internal code structuring, which differs markedly from that of Berkeley SPICE and related simulators, allows users to add new devices with only minimal knowledge of simulation algorithms, and vice-versa. We describe MAPP’s structuring and provide an overview of its capabilities. MAPP is available as open source under the GNU Public License.

4:25 pm A System-Verilog Behavioral Model for PLLs for Pre-Silicon Validation and Top-Down Design Methodology, A. Lotfy, S. Farooq, Q. Wang, S. Yaldiz, P. Mosalikanti, N. Kurd, Intel Corporation

A System-Verilog behavioral model for charge-pump PLLs based on piece-wise constant real number modeling and table lookup is presented. The proposed model exploits the sampled nature of the PLL where most of its analog behavior takes effect during phase detection. The model simulation run time takes only 1 second. Compared to transistor-level Spice simulations, the model shows a correlation of more than 97%. The PLL model is used to exercise critical features like spread-spectrum clocking and adaptive frequency system. In addition, the model was integrated in a pre-silicon validation environment and enabled catching design bugs.

4:50 pm A Mixed-Domain Modeling Method For RF Systems, Zhimiao Chen, Zhixing Liu, Lei Liao, Ralf Wunderlich, Stefan Heinen, RWTH Aachen
This paper introduces a mixed domain event driven modeling method for RF systems. The circuit behaviors are modeled in time/frequency domain adaptively combining with the equivalent baseband representation of each spectral component. Comparing to traditional baseband modeling methods or harmonic balance simulation techniques, this mixed domain method lose the requirements of relations among carrier frequencies of spectral components, and therefore can be widely used in mixed-signal circuit modeling. Furthermore, this method brings in a great simulation speed up over the simulation in passband signal abstraction, while the modeling accuracy can be guaranteed to meet the requirements of functional verifications.

5:15 pm Methods for Finding Globally Maximum-Efficiency Impedance Matching Networks with Lossy Passives, ChandraKanith R. Chappidi, Kaushik Sengupta, Princeton University

In this paper, we investigate the methods to deduce the global maximum efficiency of power transfer between two arbitrary impedances with lossy passives. This paper also proposes methods to combine this with nonlinear load-pull simulations for optimal efficiency combiner and matching network for integrated PAs. To the best of the authors’ knowledge, this is the first comprehensive analysis of globally optimal impedance transformation networks between arbitrary impedances with lossy passives.

Session 10 - Memory Advancements

Monday Afternoon, September 28, Fir Ballroom

Session Chair: Dinesh Somasekhar, Intel
Session Co-Chair: Jean-Christophe Vial, Intel Mobile Communications

Advances in solutions for memory technologies ranging from DRAM, PCRAM, STTRAM, and SRAM are topics covered in this session.

3:30 pm Introduction

3:35 pm Design Considerations of HBM Stacked DRAM and the Memory Architecture Extension (INVITED), Dong Uk Lee, Kang Seol Lee, Yongwoo Lee, Kyung Whan Kim, Jong Ho Kang, Jaejin Lee, Jun Hyun Chun, SK Hynix

Recently, the 3D stacked memory, which is known as HBM (high bandwidth memory), using TSV process has been developed. The stacked memory structure provides increased bandwidth, low power consumption, as well as small form factor. There are many design challenges, such as multi-channel operation, microbump test and TSV connection scan. Various design methodology make it possible to overcome the difficulties in the development of TSV technology. Vertical stacking enables more diverse memory architecture than the flat architecture. The next generation of HBM focuses on not only the bandwidth but also the system performance enhancement by adopting pseudo channel and 8-hi stacking. The architecture applied to the second generation HBM are introduced in this paper.


Non-resistance read metric with drift resilient nature is enhanced to be suitable for high density memory array with large parasitic time constant. Experimental results for a bank of 2Gb multi-level density are demonstrated with total read latency of 450ns.


Spin Transfer Torque Magnetoresistive RAM (STT MRAM) has uniquely attractive write performance and endurance characteristics. Nonetheless, little STT MRAM circuit hardware data has been published. This paper describes a fully-functional 90nm 8Mb STT MRAM, identifies and describes solutions to the primary circuit challenges, and includes considerable circuit hardware data.


This paper presents 64-kb 8T three-port image memory using a 28-nm FD-SOI process technology. In the test chip, the energy minimum point is a supply voltage of 0.54V at a frequency of 18.2MHz, at which 298-fJ/cycle in a write operation and 650-fJ/cycle in a read operation are achieved.

Session 11 - Advanced Techniques for Power Amplifier Transceiver Front-Ends

Session 11 - Advanced Techniques for Power Amplifier Transceiver Front-Ends
Monday Afternoon, September 28, Pine Ballroom

Session Chair: Yanjie Wang, Intel Labs
Session Co-Chair: Hua Wang, Georgia Institute of Technology

This session showcases multiple state-of-the-art designs on wireless transceiver front-end as well as fully integrated power amplifiers including a dual-band linear digital polar power amplifier, a broadband mm-wave linear power amplifier and a mm-wave switching power amplifier.

3:30 pm Introduction

3:35 pm

11-1 A Dual-Band 802.11abgn/ac Transceiver with Integrated PA and T/R Switch in a Digital Noise Controlled SoC (INVITED), Yuan-Hung Chung, Che-Hung Liao, Chun-Wei Lin, Yi-Shing Shih, Chin-Fu Li, Meng-Hsiung Hung, Ming-Chung Liu, Pi-An Wu, Jui-Lin Hsu, Ming-Yeh Hsu, Sheng-Hao Chen, Po-Yu Chang, Chih-Hao Chen, Yu-Hsien Chang, Jun-Yu Chen, Tao-Yo Chang, George Chien, MediaTech Inc.

This paper describes a dual-band 802.11abgn/ac compliant transceiver in a 4-in-1 combo connectivity SoC. It integrates the PAs, LNAs, T/R switches, and the 5GHz Balun. Due to the transmitter architecture and adaptive biasing scheme both are tailored for wide bandwidth, the 5GHz transmitter achieves 18.2dBm average output power for 802.11ac VHT80 MCS9 (Modulation and Coding Scheme 9). Within the 80MHz channel bandwidth, the IQ mismatch becomes frequency dependent, and is compensated through calibration. In the 2.4GHz transmitter, its PA load-line is adjustable. The power efficiency is thus remained similarly regardless the output power is at 20dBm for long range operation, or 8dBm for short range operation. By controlling the turn-on resistance of power island switch in digital baseband, and properly sizing the filler cap, the switching noise can be well controlled. The chip occupies 24.9mm² in 55nm 1P6M CMOS technology, where 1.3mm² is for 5GHz WLAN and 2.1mm² is for 2.4GHz WLAN/BT.

4:25 pm


This paper presents a highly linear dual-band mixed-mode polar power amplifier in CMOS. An ultra-compact single-transformer passive network provides dual-band optimum load-pull impedance matching, parallel power combining, and double even-harmonic rejection. The mixed-mode architecture leverages both digital and analog techniques to suppress the AM-AM and AM-PM distortions.

4:50 pm

11-3 A 15 GHz-Bandwidth 20 dBm P_{sat} Power Amplifier with 22% PAE in 65 nm CMOS, J. Zhao, M. Bassi, A. Mazzanti, F. Svelto, University of Pavia

To generate high output power with high efficiency over large bandwidth, a design technique to embed classical coupled resonators networks into power splitters and combiners is presented for the first time. The realized PA shows 15 GHz bandwidth with 30 dB gain, 20 dBm output power and 22% PAE.

5:15 pm

11-4 A 28 GHz Inverse Class-F Power Amplifier with Coupled-Inductor based Harmonic Impedance Modulator, S. Y. Mortazavi, Kwang-Jin Koh, Virginia Tech

This paper presents a 28 GHz class-F-1 power amplifier in 0.13-µm SiGe BiCMOS technology. The PA adopts a coupled-inductor based harmonic impedance modulator in order to terminate 2nd and 3rd harmonic load impedances appropriately for class-F-1 operation. The coupled coils essentially provide frequency-dependent inductance that is optimal to resonate out 2nd and 3rd harmonic reactive impedance. The PA achieve 40-42% PAE over 27.5 GHz to 29 GHz, peak 42% PAE at 28 GHz with 50 mW OP-1dB power, one of the highest PAEs ever reported in silicon-based PAs. At 6-dB backoff output power, the PAE is as high as 20%. Psat is 16.6 dBm.

Monday Afternoon, September 28, Cedar Ballroom

Session Chair: Robert Aitken, ARM
Session Co-Chair: Tetsuya Iizuka, Univ. of Tokyo

This embedded tutorial discusses recent advances in the field of large area electronics including organic and thin film transistors in addition to CMOS.

3:30 pm Introduction

3:35 pm

12-1 Recent Development in High-Mobility Organic Field-Effect Transistors, Takafumi Uemura, Osaka Univ.

4:25 pm

12-2 A hybrid Large-Area Electronics: A Solution for Low-Cost Mass-Parallel Operations, Reza Chaji, Ignis Innovations

5:15 pm Build Your Own Chip: Plastic Ics via Printed Electronics, Lucian Shifren, ARM
Session 13 - Panel

Monday Afternoon, September 28, Silicon Valley Ballroom

3:30 pm  What is 5G?

Organizer(s): Stacy Ho (MediaTek)
Moderator name and affiliation: Ramesh Harjani (University of Minnesota)

Panelists:
Chris Hull (Intel)
Steven Hong (Kumu Networks)
Payam Heydari (UC Irvine)
Sohrab Emami (Co-founder, SiBEAM)

The push to increase wireless data capacity up into the Gb/s realm is gaining speed and technologists around the world are racing to define what 5G will be. This panel features a few experts that will try to answer the question, “What is 5G?” Among the topics that will be discussed are mmWave, integration with WLAN, MIMO, and interference cancellation.

Poster Session

5:00 pm – 7:00 pm
Siskiyou/Cascade Ballroom

M-1 A Linear Transconductance Amplifier with Differential-Mode Bandwidth Extension and Common-Mode Compensation, Derui Kong, Sang Min Lee, Shahin Mehdizad Taleie, Michael Joseph McGowan, Dongwon Seo, Qualcomm Technologies, Inc

A transconductance amplifier with extended bandwidth, which is a critical block in various applications including amplifiers, filters and DACs is presented. The presented technique introduces a differential-mode negative capacitance while introduces the common-mode positive capacitance such that it extends the differential-mode bandwidth and compensates the common-mode stability. The proposed transconductance amplifier has been implemented for a DAC in CMOS 20nm to improve the distortion performance as a negative transconductance circuit, but the proposed technique is applicable to the wide range of circuits with a transconductor.

M-2 Low Power Analog Circuit Techniques in the 5th Generation Intel CoreTM Microprocessor (Broadwell), P. Mosalkanti, N. Kurd, C. Mozak, T. Oshita, Intel Corporation

Fabricated on a 14nm process technology node, the 5th generation CoreTM processors improve energy efficiency over the previous 22nm generation by up to 2.5x. Numerous optimizations in the analog circuits contributed - lower PLL Vmin, 150mV lower clock distribution Vmin, 3x DDR power reduction, 10x lower thermal sensor power and more.

M-3 A Compact, High Linearity 40GS/s Track-and-Hold Amplifier in 90nm SiGe Technology, D. Lal, M. Abbasi, D.S. Ricketts, North Carolina State University

We report a 40GS/s Track and Hold Amplifier in 90nm SiGe HBT technology with ENOB>4.9. Up to 19GHz input, SFDR3>68dB, THD3<-31dB and IIP3>4dBm are measured with 560mW consumed over 0.03mm^2 active die area. Linearity is better than existing SiGe and CMOS THAs at 40GS/s and 50GS/s and comparable to 50GS/s InP designs for less than half the power consumption.

M-4 A Seizure-detection IC Employing Machine Learning to Overcome Data-conversion and Analog-processing Non-idealities, Jintao Zhang, Liechao Huang, Zhao Wang, and Naveen Verma, Princeton University

A seizure-detection system is presented wherein the analog frontend performs data conversion and feature extraction with greatly reduced accuracy requirements. A machine-learning algorithm enables retraining of a classification model to compensate feature errors, restoring performance from 443 to 4 false alarms (i.e., at the level of the baseline system).

M-5 A 550μm^2 CMOS Temperature Sensor Using Self-Discharging P-N Diode with +/-0.1°C (3σ) Calibrated and +/-0.5°C (3σ) Uncalibrated Inaccuracies, G. Chowdhury, A. Hassibi*, Synaptics, *University of Texas at Austin

A 550μm^2 temperature sensor with a p-n diode in a first-order Δ-Σ loop is presented. It offers calibrated inaccuracy of ±0.1°C and uncalibrated inaccuracy of ±0.5°C over the measured 35°C-100°C range. This sensor is optimized to implement a distributed thermal monitoring system in large SoCs operating typically above 30°C.

M-6 A 16-channel, 1-Second Latency Patient-Specific Seizure Onset and Termination Detection Processor with Dual
An Eight Channel Analog-FFT Based 450MS/s Hybrid Filter Bank ADC With Improved SNDR for Multi-Band Signals in 40nm CMOS, Hundo Shin, Rakesh Kumar Palani, Anindya Saha, Fang-Li Yuan*, Dejan Markovic*, Ramesh Harjani, University of Minnesota, *University of California Los Angeles

We present a complete implementation of a hybrid filter bank ADC based on an analog-FFT. The proposed structure enables the signal in each channel of the wide band system to be separately digitized using the full dynamic range of the ADC. The prototype is implemented in 40nm CMOS process.

A 14-bit 0.17mm² SAR ADC in 0.13μm CMOS for High Precision Nerve Recording, Anh Tuan Nguyen, Jian Xu, Zhi Yang, National University of Singapore

This paper presents a high-resolution, area- and power-efficient SAR ADC for high-precision nerve recording. It features a new “half-split” DAC array with integrated digital calibrations for automatic estimation and calibration of capacitor mismatches. As a result, the ADC precision can be substantially improved given the constraints on area and power.

A 0.04-mm² 0.9-mW 71-dB SNDR Distributed Modular ΔΣ ADC with VCO-based Integrator and Digital DAC Calibration, Y. Yoon, K. Lee, S. Hong, X. Tang, L. Chen, N. Sun, University of Texas at Austin

This paper presents a low-power and small-area VCO-based closed-loop ADC with two highlights. First, the ADC has a distributed modular architecture, which allows the ADC to be easily reconfigured for other resolution specifications. Second, a novel digital DAC mismatch calibration technique is proposed. It ensures high linearity in the presence of large DAC mismatches.

A 16nm Configurable Pass-Gate Bit-Cell Register File for Quantifying the $V_{min}$ Advantage of PFET versus NFET Pass-Gate Bit Cells, Jhoon Jeong, Francois Atallah, Hoan Nguyen, Josh Puckett, Keith Bowman, David Hansquine, Qualcomm Technologies, Inc

A 16nm configurable pass-gate bit-cell register file allows a direct comparison of NFET versus PFET pass-gate bit cells for early technology evaluation. The configurable pass gate enables either a transmission-gate (TG), an NFET pass gate, or a PFET pass gate. From silicon test-chip measurement, the register file with PFET pass-gate bit cells achieves a 33% minimum supply voltage ($V_{min}$) reduction in a 16nm FinFET technology and a 40% $V_{min}$ reduction in an enhanced 16nm FinFET technology as compared to a register file with NFET pass-gate bit cells. Test-chip measurements highlight the superior benefits of the PFET drive current relative to the NFET drive current at low voltages. The $V_{min}$ improvement with a PFET pass-gate bit cell represents a paradigm-shift from traditional CMOS circuit-design practices.

Custom 6-R, 2- or 4-W Multi-Port Register Files in an ASIC SOC with a DVFS Window of 0.5 V, 130 MHz to 0.96 V, 3.2 GHz in a 28-nm HKMG CMOS Technology, Henry Hsieh, Sang H. Dhong, Cheng-Chung Lin, Ming-Zhang Kuo, Kuo-Feng Tseng, Ping-Lin Yang, Kevin Huang, Min-Jer Wang, and Wei Hwang*, TSMC, *National Chiao-Tung University

We describe custom 6R, 2/4W general-purpose register files (GRF) in an ASIC-based SOC, which has roughly a 2-3X smaller area, 2X faster speed, and 5X lower power than a logic-synthesized version. Hardware showed a DVFS window of 0.5 V @ circuit, 130 MHz to 0.96 V, 3.2 GHz.


A 14.8μVRMS integrated-noise (10Hz-100kHz) LDO using switched-RC sample-and-hold bandgap and current-mode chopped, any-load capacitor stable error amplifier in 0.25µm CMOS process is presented. It delivers maximum load of 100mA with dropout of 230mV and IQ of 40µA. It achieves PSR of 50dB at 10kHz for programmable output voltage of 1.5-3.3V.

A Scalable and Reconfigurable 2.5D Integrated Multicore Processor on Silicon Interposer, Jie Lin, Shikai Zhu, Zhiyi Yu, Dongjun Xu*, Sai Manoj P.D.*, Hao Yu*, Fudan University, *Nanyang Technological University

This paper presents a 2.5D multicore processor, which is flexible to be organized into various multi-chip systems to meet different application requirements. The 2.5D I/O supports 12 way full-duplex communication each by a pair of 8Gbps SerDes, achieving a bandwidth of 24Gb/s. The system consumes 1.08W in GF 65nm process.


The implementation of the SubBytes (or S-Box) step of the AES algorithm significantly contributes to the area, delay, and power of AES accelerators. Unlike typical logic gate S-Box implementations, we use full-custom 256x8-bit ROMs, which significantly improve performance and efficiency. We implemented a fully-unrolled, pipelined AES-128 encryption accelerator using ROM-based S-Boxes in 65nm bulk CMOS which operates at 2.2Ghz and consumes 523mW at 1.0V, 27C. In counter-mode operation (CTR), the throughput is 275Gbps, which is 5.2x higher than the highest ever reported.
in the literature to our knowledge.

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<tr>
<th>M-15</th>
<th>Efficiency Improvement Techniques for RF Power Amplifiers in Deep Submicron CMOS, Aritra Banerjee, Rahmi Hezar, Lei Ding, Texas Instruments</th>
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<tr>
<td></td>
<td>Integration of RF power amplifier in CMOS technology can help to reduce total solution cost and achieve small form factor in modern communication systems. This paper reviews recent developments in CMOS based PA architectures including PWM based digital transmitter and outphasing power amplifier and presents a multi-mode outphasing PA.</td>
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<th>M-16</th>
<th>Wireless Synchronization of mm-wave Arrays in 65nm CMOS, Charles Chen, Aydin Babakhani, Rice University</th>
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<td></td>
<td>This paper presents the first wireless synchronization of a mm-wave array, eliminating the need for connecting wires between the array elements. Wireless injection locking is successfully demonstrated and a 3dB bandwidth of 400Hz at a carrier frequency of 50GHz is achieved (frequency stability of 8ppb). The chip includes two on-chip antennas, a power amplifier, a phase-shifter, buffer amplifiers, and a VCO. The chip is fabricated in a 65nm CMOS process and occupies an area of 1.7mm × 3.8mm.</td>
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<th>M-17</th>
<th>390-640MHz Tunable Oscillator Based on Phase Interpolation with -120dBc/Hz In-Band Noise, Xu Meng, Lianhong Zhou*, Fujiang Lin, Chun-Huat Heng*, University of Science and Technology of China, *National University of Singapore</th>
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<td>A tunable oscillator based on phase interpolation has been studied. It utilizes delta sigma modulator to randomly select between the multi-phase outputs of a digitally-controlled injection-locked ring oscillator, thus achieving a low phase noise tunable high frequency reference that can be applied to normal integer-N PLL.</td>
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<th>M-18</th>
<th>A 0.1-5.0GHz Self-Calibrated SDR Transmitter with -62.6dBc CIM3 in 65nm CMOS, Yun Yin, Yanqiang Gao, Zhihua Wang, Baoyong Chi, Tsinghua University</th>
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<td>A 65nm 0.1-5.0GHz self-calibrated SDR transmitter is presented. A complete self-calibration scheme is proposed to alleviate the non-ideal effects, including RF operation frequency deviation, output power control, LO leakage and image suppression. A power mixer RF front-end and a V-I converter with 3rd-order nonlinearity cancellation are adopted to improve the CIM3 performance. A Class-AB/F dual-mode PA is integrated for narrowband applications.</td>
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<th>M-19</th>
<th>A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs, J. Zhu, P. R. Kinget, Columbia University</th>
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<tr>
<td></td>
<td>A field-programmable noise-canceling wide-band receiver front end with high performance LNTAs is presented. The common-source (CS) and common-gate (CG) LNTAs are split into several cells whose bias point can be individually programmed in class AB or C yielding a highly linear hybrid class-AB-C LNTA. The 40nm LP CMOS receiver prototype can be programmed on the fly to adapt to different RF environments; it was tested in a low noise mode, a high linearity mode and a low power mode. Across these modes, the receiver has maximum gain of 53dB, a minimum NF of 2.2dB, a maximum B1dB of +11dBm, and a maximum OB-IIP3 of +21dBm; the signal path consumes between 15 and 40mA from a 2.5V supply and the LO current varies from 2.2 to 20mA from a 1.1V supply across operating frequencies. The measured LO emission at the antenna port is &lt;-84dBm.</td>
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