Education Session Schedule

Educational Session 1 -
Monday Morning, September 28, Cedar Ballroom

Session Chair: Tim Hancock, Massachusetts Institute of Technology
Session Co-Chair: Eric Naviasky, Cadence Design

10:00 am  Low Dropout Regulators, Pavan Hanumolu, University of Illinois, Urbana-Champaign

This tutorial presents the design, analysis, and practical circuit implementation of low dropout regulators (LDOs). We begin with a review of traditional LDO regulator topologies and evaluate their key performance metrics such as dropout voltage, power supply rejection ratio, load and line regulation accuracy, settling time in the presence of load step, current efficiency, and stability. Following this, we describe alternate LDO architectures and illustrate how one can tradeoff some of the aforementioned performance metrics. We conclude with case study of a few state-of-the-art high performance LDOs.

Pavan Hanumolu is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, in 2006, where he subsequently served as a faculty member till 2013. Dr. Hanumolu's research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.

Educational Session 2
Monday Afternoon, September 28, Cedar Ballroom

Session Chair: Larry Nagel
Session Co-Chair: Larry Clark

1:30 pm  Behavioral Modeling Options For Balancing Verification Coverage and Credibility, Jess Chen, Qualcomm

The purpose of verification is to reduce the risk of silicon not meeting performance specifications or worse yet, not functioning. Since the silicon does not yet exist, verification depends on simulations. Simulations in turn depend on models. In verification terms, the classical modeling tradeoff between speed and accuracy translates into a tradeoff between test coverage and model credibility (or validity). Transistor-level models produce the most credible simulations but slow run times and convergence problems severely limit test coverage. At the other extreme, a high level flat model quickly simulates all required tests but is least credible because the high level of abstraction greatly increases the chances for un-modeled circuit bugs and other relevant omitted behaviors. A “good” modeling boundary balances coverage and credibility. The balance is subjective because it depends on schedule, available resources, and acceptable risk. Given how strongly verification depends on the overall modeling strategy, it helps to have as many modeling options as possible. This tutorial describes a few modeling methods to balance coverage and credibility.

Jess Chen manages two groups of radio verification engineers at Qualcomm. Besides his relatively recent managerial duties, Jess has spent the last 20 years modeling RF
systems and components at various companies. Before that, he spent 15 years at Lockheed Martin modeling and analyzing space craft power systems, motor drives, and unusual test equipment. Jess earned a BA in physics and applied math from UC Berkeley in 1977, an MSEE from San Jose State in 1982, the degree of engineer in control theory from Stanford University in 1985, and an MSME from Santa Clara University in 1991.

Educational Session 3
Tuesday Morning, September 29, Cedar Ballroom

Session Chair:
Session Co-Chair:

9:00 am TBD, Bram Nauta

Educational Session 4
Tuesday Morning, September 29, Cedar Ballroom

Session Chair: Howard Luong, Hong Kong University of Science & Tech.
Session Co-Chair: Foster Dai, Auburn University

11:00 am Phase-Locked Frequency Synthesis and Modulation for Modern Wireless Transceivers, Woogeun Rhee, Institute of Microelectronics, Tsinghua University, Beijing, China

Frequency synthesis and modulation by the DS fractional-N PLL are essential in modern wireless transceivers. In addition to loop parameter variability, leakage current, and matching problems, the DS fractional-N PLL needs to deal with quantization noise and nonlinearity in consideration of phase noise, spur, and settling time. In this talk, various fractional-N PLL architectures (analog/digital/hybrid) and recent circuit techniques for mitigating quantization and nonlinearity will be discussed. Also, PLL-based modulation methods (1-point/2-point/2'-point) will be overviewed.

Woogeun Rhee received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1991, the M.S. degree in electrical engineering from the University of California, Los Angeles, in 1993, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, Newport Beach, CA, where he was a Principal Engineer and developed low-power, low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY and worked on clocking area for high-speed I/O serial links, including low-jitter phase-locked loops, clock-and-data recovery circuits, and on-chip testability circuits. In August 2006, he joined the faculty as an Associate Professor at the Institute of Microelectronics, Tsinghua University, Beijing, China, and became a Full Professor in December 2011. His current research interests include clock/frequency generation systems for wireline and wireless communications and low-power transceiver systems for wireless body area networks. He currently holds 20 U.S. patents. Rhee served as an Associate Editor for IEEE Transactions on Circuits and Systems Part-II: Express Briefs (2008-2009) and a Guest Editor for IEEE Journal of Solid-State Circuits Special Issue in November 2012 and November 2013. He is currently an Associate Editor for IEEE Journal of Solid-state Circuits. He is also a member of the Technical Program.
Committee for several IEEE conferences including ISSCC, CICC, and A-SSCC.

Educational Session 5  
Tuesday Afternoon, September 29, Cedar Ballroom  

Session Chair: Elad Alon, University of California Berkeley  
Session Co-Chair: Azita Emami, CalTech  

2:00 pm  
Supply noise induced jitter modeling and optimization for high-speed interfaces,  
Dan Oh, Altera  

The supply noise impact plays a major role in designing modern high-performance SOC or FPGA devices. A conventional power distribution network design to minimize supply noise can lead to significant overdesign and often times can no longer be implemented in an effective way. Optimal power distribution network can be designed based on modeling supply noise induced jitter and its impact on system-level performance, instead of focusing on noise reduction. This talk presents the key issues and challenges in high-speed link interfaces due to supply noise, the basics of supply noise induced jitter modeling, and unique design techniques for different signaling applications such as memory interfaces, serial links, and digital logic paths.

Dan Oh is a Signal and Power Integrity (Si/Pi) Architect at Altera where he is responsible for leading cross functional Si/Pi co-design teams including IC design, packaging, and product engineering as well as driving the overall Si/Pi technical direction. Dr. Oh was most recently a Technical Director at Rambus Inc. where he defined the signaling roadmap, supported system definition of new product proposals, and drove IP development for innovative signaling solutions. He has over 25 years of experience in the area of signal and power integrity. Dr. Oh received his Ph.D. in Electrical Engineering from the University of Illinois at Urbana-Champaign. He has numerous patents and papers in the areas of high-speed I/O modeling, simulation, and design. He is the lead author of the book High-speed Signaling: Jitter Modeling Analysis, and Budgeting, and also serves on the technical program committees of leading conferences such as IEEE EPEPS, IEEE ECTC, IEEE EMC SIPI, and IBM DesignCon.

Educational Session 6  
Tuesday Afternoon, September 29, Cedar Ballroom  

Session Chair: Jay Wang, Intel  
Session Co-Chair: Byunghoo Jung, Purdue University  

4:00 pm  
MMIC for 5G, Ali Sadri -- Intel Corporation  

Increasing the capacity of next-generation backhaul and access networks is becoming one of the most challenging tasks of the industry this decade. As traditional mechanisms to increase spectral efficiency approach their theoretical limits, new and disruptive techniques are needed to satisfy the growing demand of mobile data traffic. Consequently, the fifth generation (5G) cellular access system is expected to make extensive use of small cells to increase the density and capacity by several hundred times in comparison with 4G systems. Not only cellular access, wireless backhaul
solutions require increased density and capacity. While considerable focus has been rightly put into exploiting licensed frequency bands below 6 GHz, the vast amount of licensed frequency spectrum in millimetre wave (mmWave) bands has seen little use by cellular access systems despite holding far greater potential for enhancing capacity. Not only licensed spectrum, unlicensed mmWave spectrums (57-63GHz) can be considered for wireless backhaul solutions. This presentation introduces novel architectures, beamforming, RFIC and manufacturing for mmWave capable small cells (MCSCs) with modular antenna arrays for backhaul and access. This architecture makes use of heterogeneous network components combined with the use of mmWave based technologies for the backhaul, fronthaul and access. We show that MCSCs can significantly increase capacity and density for backhaul and access systems.

Dr. Ali Sadri is Sr. Director of mmWave Standards and Advanced Technologies at Intel Corporation. His Professional work started at IBM, who was responsible for communications standards, in year 1990 and a Visiting Professor at the Duke University through year 2000. During years 2000-2002 he joined BOPS Inc., a startup company specialized in programmable DSP's as the Sr. Director of the Communications and Advanced Development. In 2002 Ali joined Intel Corporation's Mobile Wireless Division where he initiated and lead the standardization of the next generation High Throughput WLAN at Intel that became the IEEE 802.11n standards. Later Ali founded and led the Wireless Gigabit Alliance since 2008 that created the ground breaking WiGig 60 GHz technology. In June 2013 WiGig Alliance merged with WiFi Alliance to advance and certify the WiGig programs within WiFi alliance framework. Currently Ali is leading the mmWave advanced technology development that includes the next generation WiGig standards and mmWave technology for 5G cellular systems for future backhaul and access networks. Ali holds more than 100 Issued and pending patent applications in wired and wireless communications systems.

Educational Session 7
Wednesday Morning, September 30, Cedar Ballroom

Session Chair: John McNeill, Worcester Polytechnic Institute
Session Co-Chair: Mohammad Ranjbar, Inphi Corporation

9:00 am  SAR ADCs in time-interleaved converter arrays, Ron Kapusta, Analog Devices

The time-interleaved ADC was first published more than 30 years ago, yet recently has experienced a surge in interest, as the demand for increased bandwidth has outstripped the performance capability of existing single-core ADCs. Concurrent with this trend has been recent focus on the SAR ADC architecture. As it turns out, the SAR ADC is particularly well-suited for use in time-interleaved arrays. This tutorial talk will review the use of highly-parallel and time-interleaved converter arrays, including both the benefits provided to and the additional constraints placed upon the system. Similarly, the SAR architecture will be examined, demonstrating how its trade-offs, as compared to other ADC architectures, interact almost synergistically with the time-interleaved configuration. Finally, a number of case studies will be presented to highlight some recent advances in achieving very high data throughput while maintaining the required accuracy. Enabling design and calibration techniques will be covered.

Ron Kapusta received the B. S. and M. Eng. degrees from the Massachusetts Institute of Technology, in 2001. Upon graduation, he joined Analog Devices, designing data converters and sensor interface circuits for multiple channel data acquisition systems. More recently, he has been with the Automotive Technology group, working on signal
acquisition for MEMS-based inertial systems. Ron has presented at multiple IEEE conferences in addition to journal papers. He holds more than 40 U.S. and international patents and won the 2013 JSSC Best Paper award. He has served on the technical program committees for CICC and VLSI Circuits.

Educational Session 8
Wednesday Afternoon, September 30, Cedar Ballroom

Session Chair: Jay Wang
Session Co-Chair: Byunghoo Jung

1:30 pm Resonant Wireless Power Transfer: Technology and Integration Roadmap,
Francesco Carobolante, Qualcomm

The promise of Resonant Wireless Power Transfer to enable seamless user experience while charging a variety of mobile devices with differing power requirements (from wearable and mobile devices to tablets and notebooks) is finally reaching maturity. While the specifications are now available and hardware is shown to be capable of charging devices from less than 1W up to 50W, the process of integration is now on the way, in order to address coexistence of the technology with the rest of the system, as well as size and cost constraints. After an introduction to Magnetic Resonance Wireless Power Transfer technology, this presentation will provide an overview of the challenges and trade-offs that led to the development of its specifications (including frequency selection, efficiency and thermal requirements, and other regulatory and use case considerations). Circuit implementations for both Transmitter and Receiver will be introduced, with a focus on new silicon and packaging technologies that enable high levels of integration, especially in space-constrained wearable devices and high power applications like notebooks.

Francesco Carobolante is Vice President of Engineering at Qualcomm Incorporated. In this position, he has been responsible for the development of products and technologies for mixed signal Integrated Circuits (primarily in Power Management and analog subsystems). He is currently leading the development of Wireless Power Transfer technology and its standardization through A4WP (the Alliance for Wireless Power). Prior to joining Qualcomm, he held positions at STMicroelectronics, Tripath Technology and Fairchild Semiconductors, developing analog, power, and MEMS based mixed signal products. He holds more than 50 patents and has published several papers on power, mixed signal and system design. He received an Electrical Engineering and PE degrees from the University of Padova in Italy, and a MSEE from UCLA.